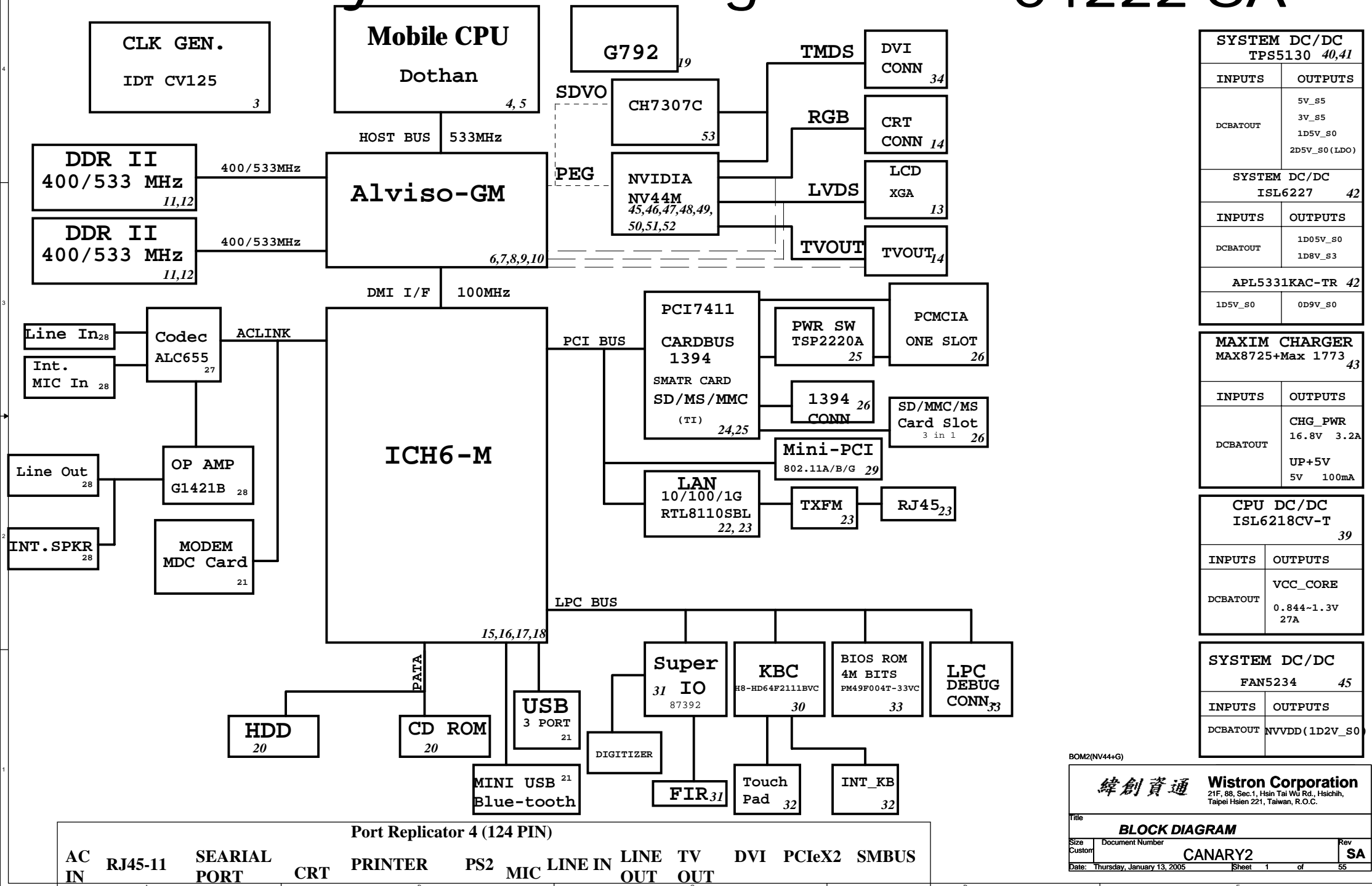


Canary2 Block Diagram

04222-SA



SYSTEM DC/DC TPS5130 40,41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5 1D5V_S0 2D5V_S0(LDO)
SYSTEM DC/DC ISL6227 42	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
APL5331KAC-TR 42	
1D5V_S0	0D9V_S0
MAXIM CHARGER MAX8725+Max 1773 43	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 16.8V 3.2A UP+5V 5V 100mA
CPU DC/DC ISL6218CV-T 39	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A
SYSTEM DC/DC FAN5234 45	
INPUTS	OUTPUTS
DCBATOUT	NVVDD(1D2V_S0)

BOM2(NV44+G)

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Rev
BLOCK DIAGRAM	SA
Size	Document Number
Custom	CANARY2
Date	Sheet
Thursday, January 13, 2005	1 of 55

Alviso Strapping Signals
and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott 1 = Dothan (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH FWORK In signal.

CY28411ZC Spread Spectrum
Select

SS3	SS2	SS1	Spread Mode	Spread Amount%
0	0	0	Down	0.8
0	0	1	Down	1.25
0	1	0	Down	1.75
0	1	1	Down	2.5
1	0	0	Center	+~0.3
1	0	1	Center	+~0.5
1	1	0	Center	+~0.8
1	1	1	Center	+~1.25

PCI Routing

	IDSEL	IRQ	REQ/GNT
7411	25	B.F.G	0
MiniPCI	21	E	1
LAN	23	E	2

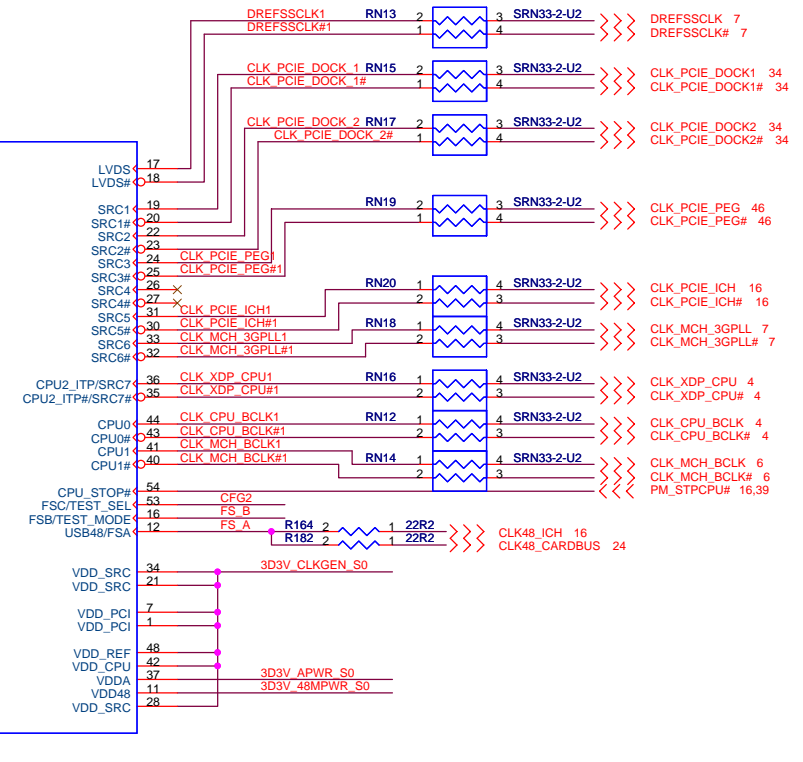
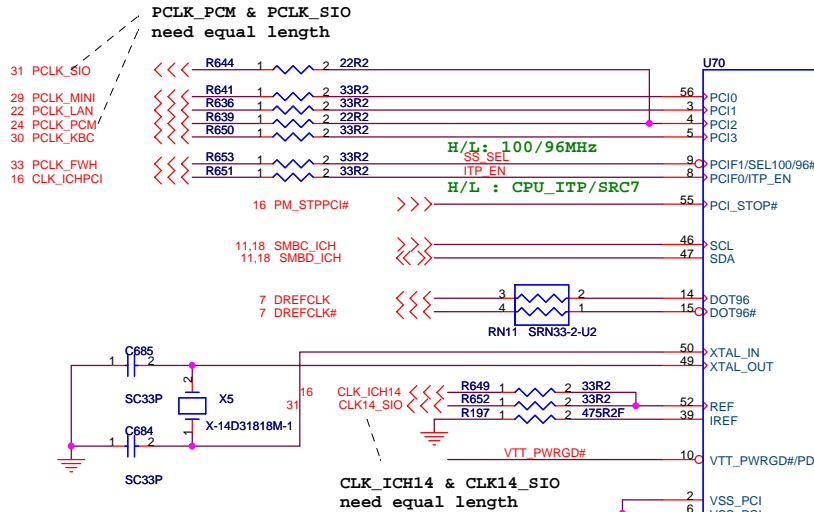
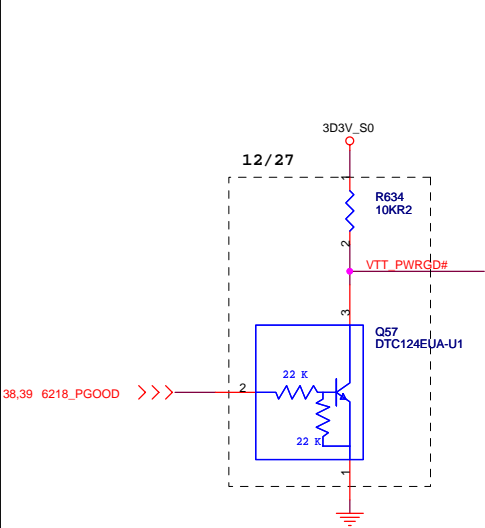
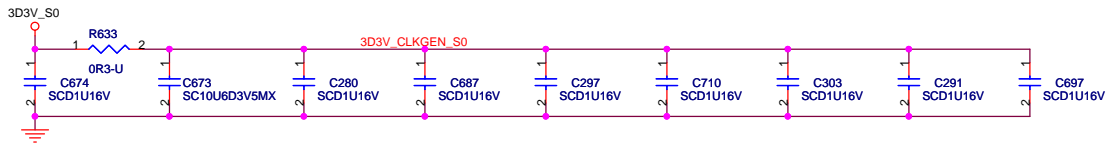
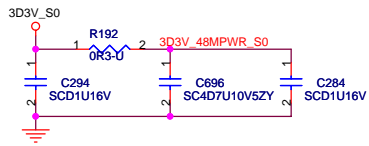
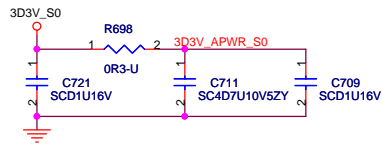
ICH6-M Integrated Pull-up
and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

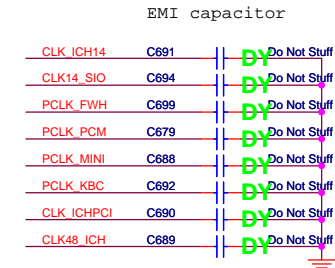
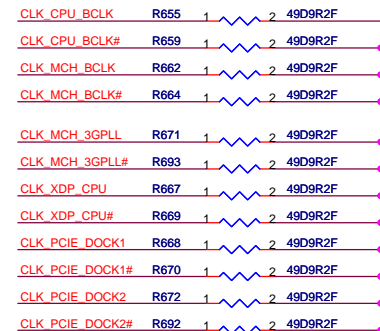
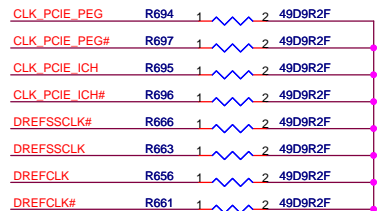
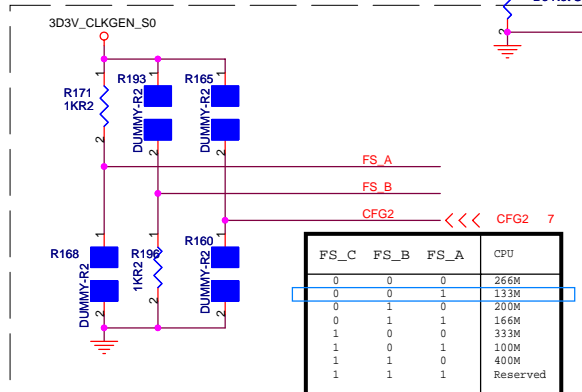
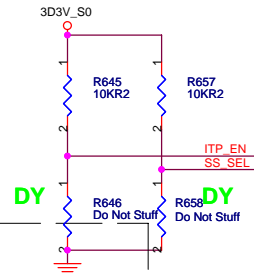
ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series
Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------



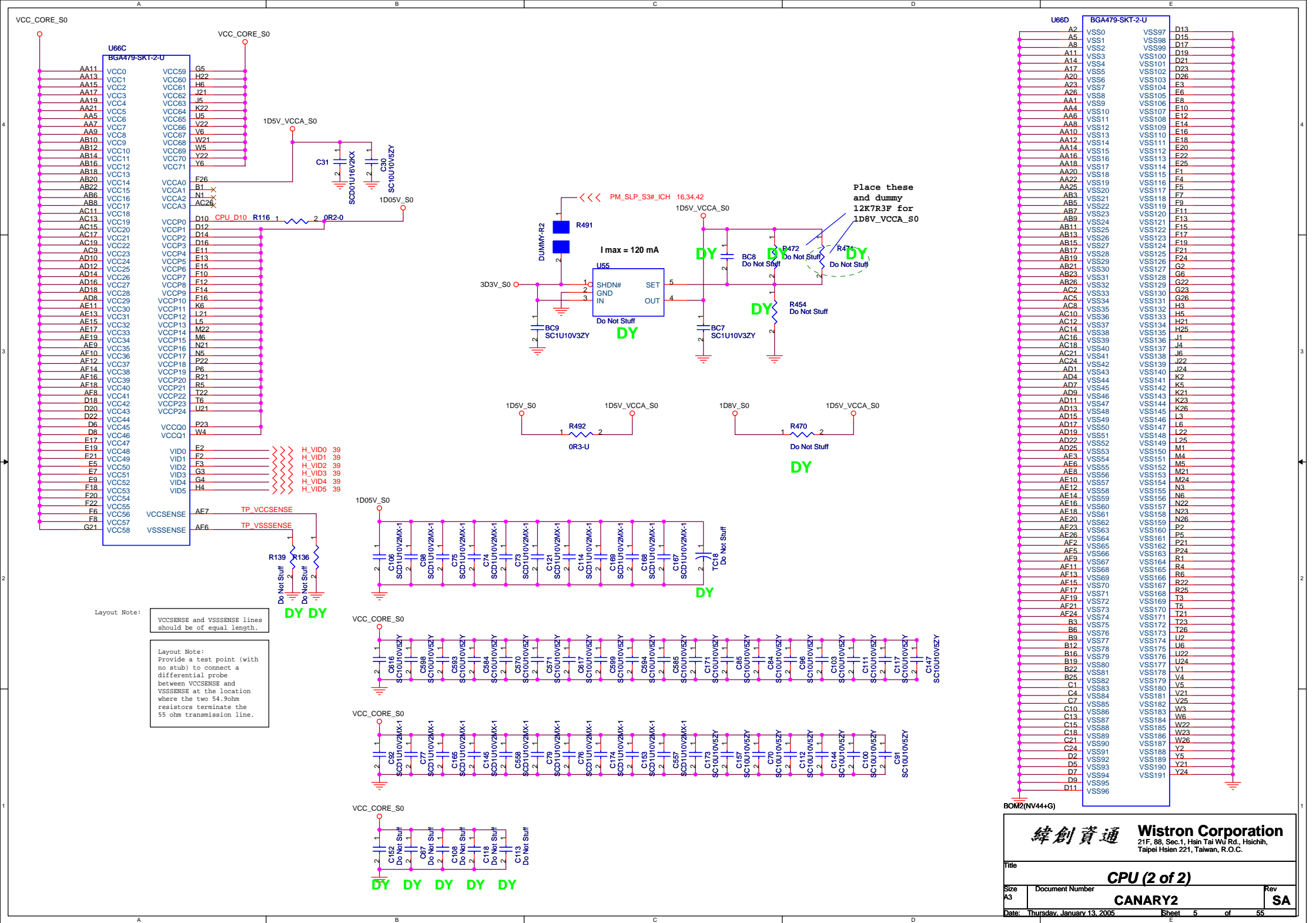
IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z

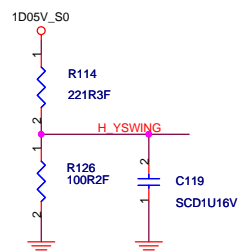


BOM2(NV44+G)

Title		Rev	
Clock Generator - IDT125		SA	
Size A3	Document Number	CANARY2	
Date: Thursday, January 13, 2005	Sheet 3	of 55	

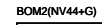
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.





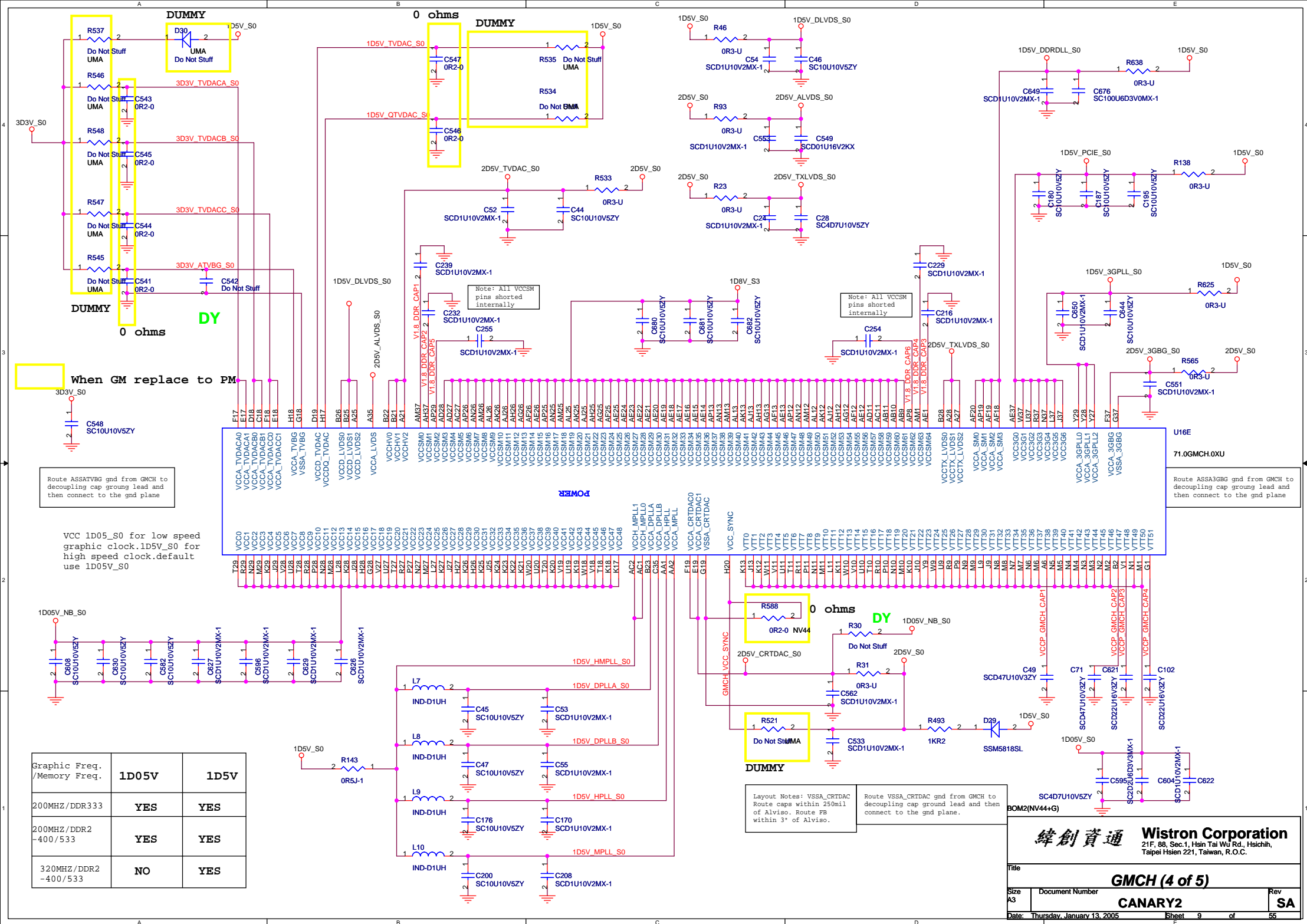
WWW.AliSaler.Com

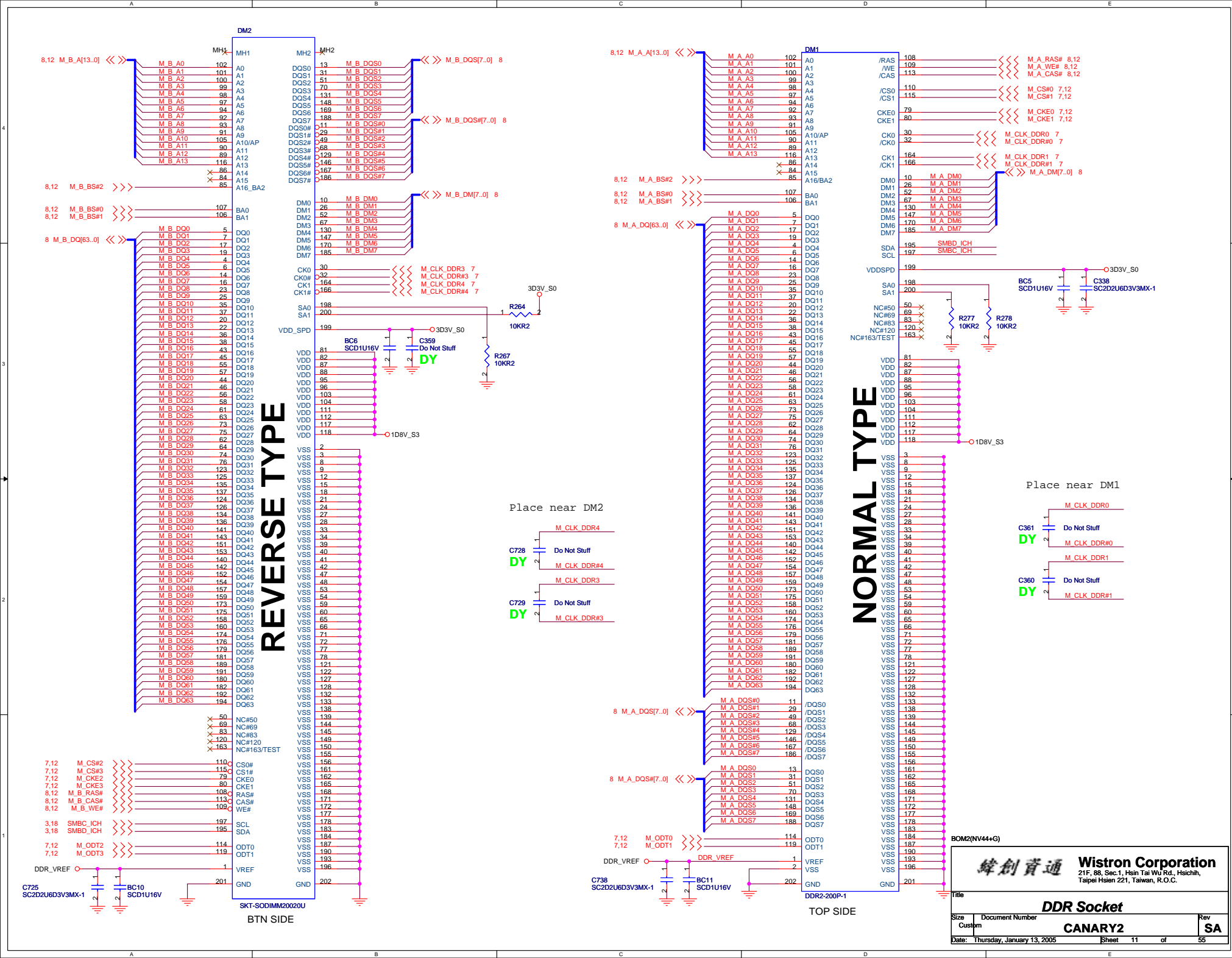
Alviso will provide SDVO_CTRLCLK
and CTRLDATA pull downs on-die



Title			
GMCH (2 of 5)			
Size Custom	Document Number		Rev
	CANARY2		SA
Date:	Thursday, January 13, 2005		Sheet 7 of 55

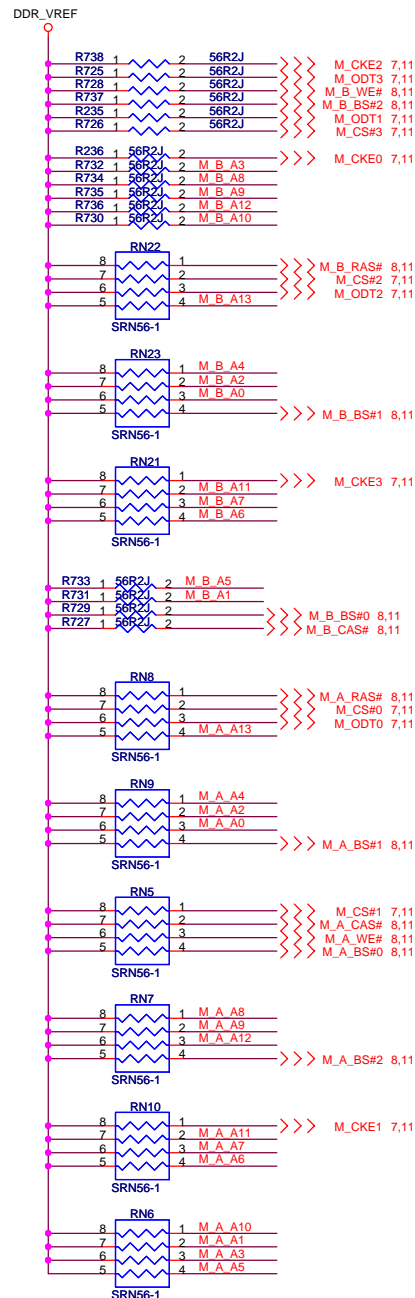
Place near U104





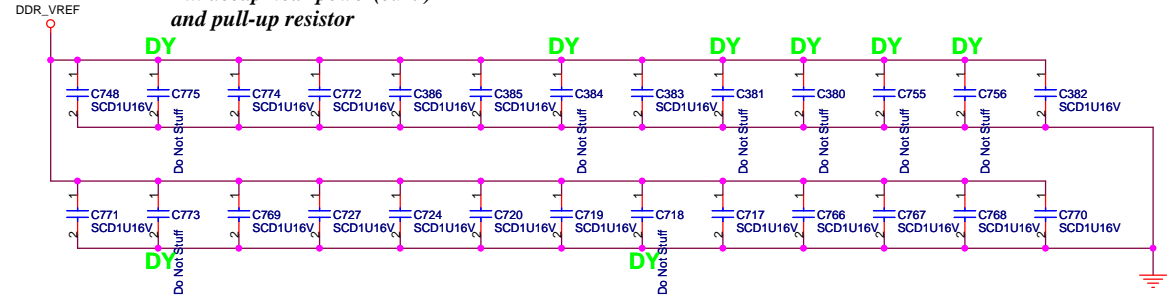
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

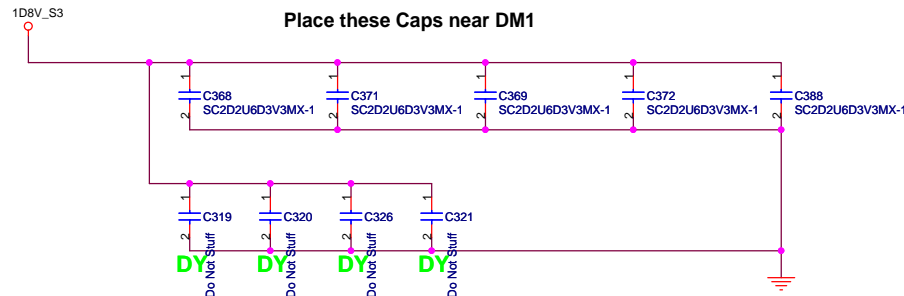


Decoupling Capacitor

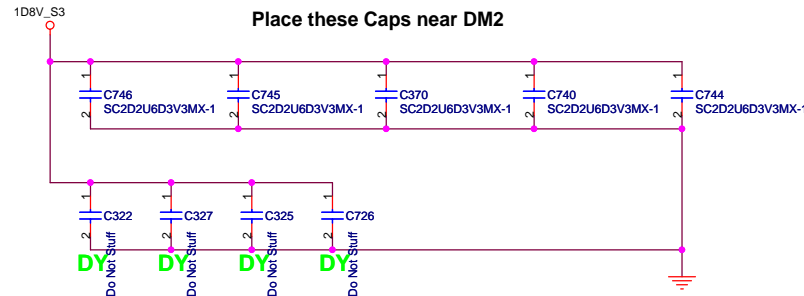
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2

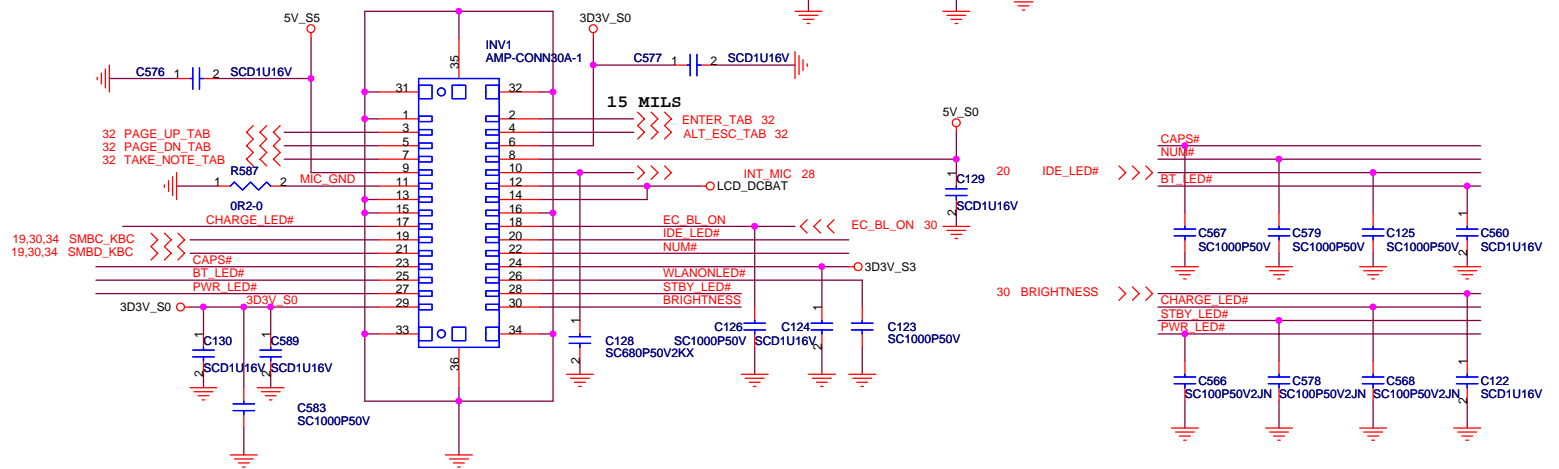
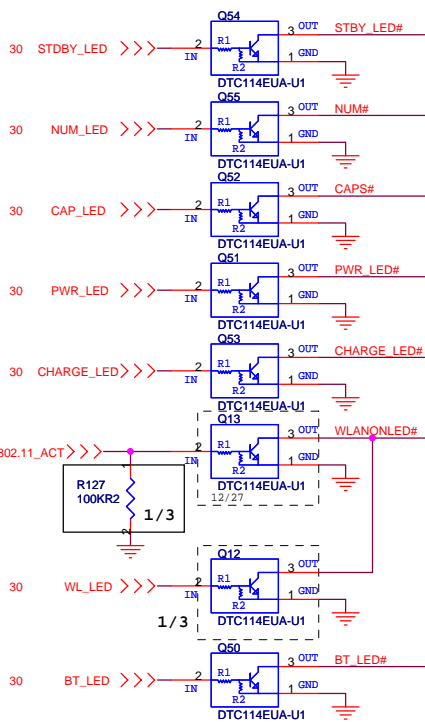


BOM2(NV44+G)

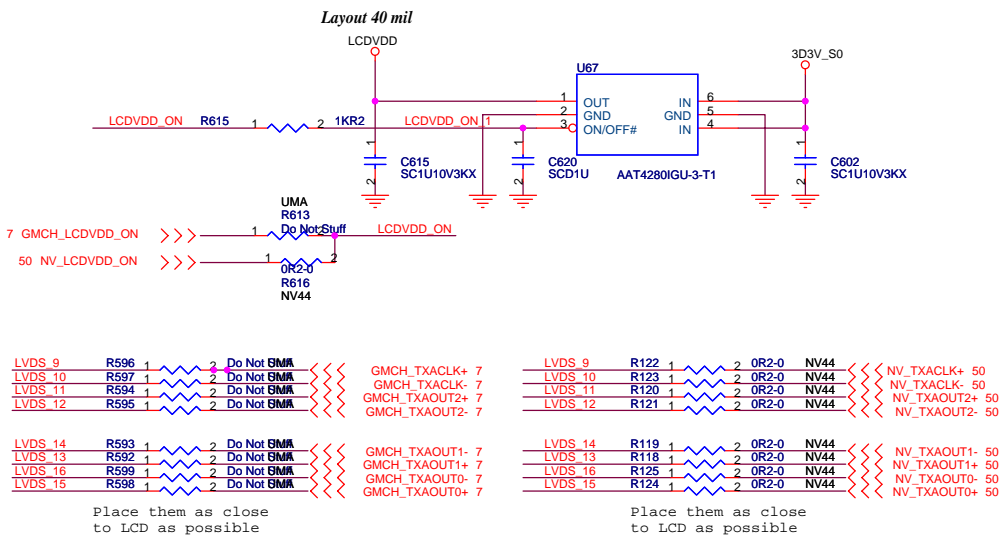
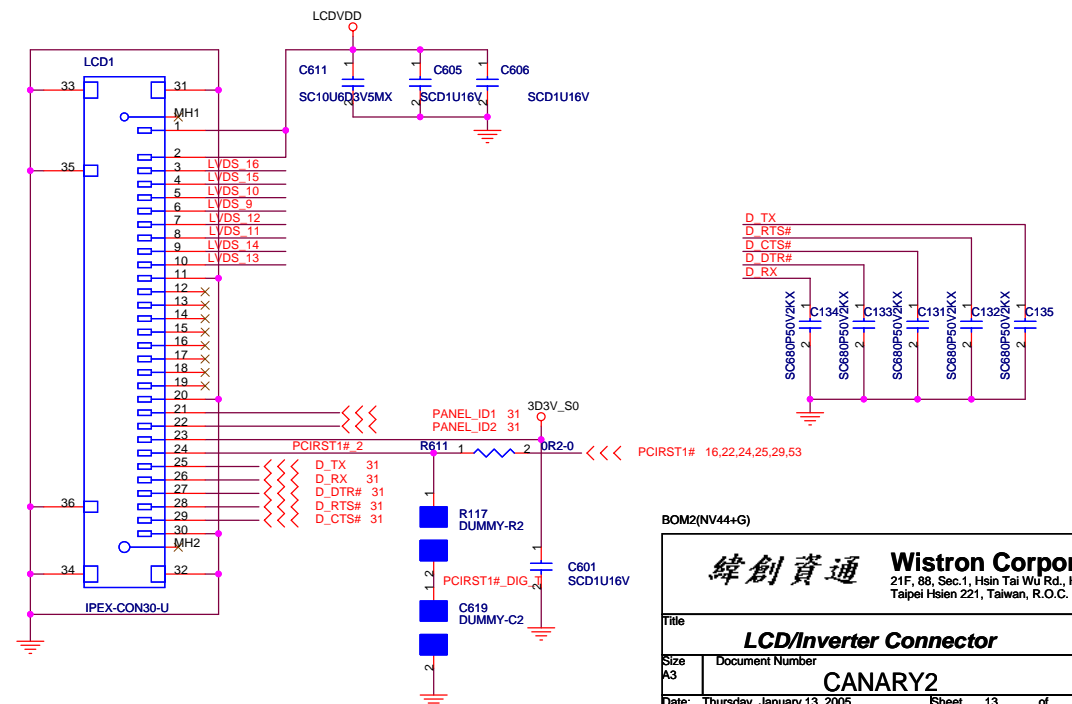
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			DDR2 Termination Resistor
Size	Document Number	CANARY2	
A3		Rev	SA
Date:	Thursday, January 13, 2005	Sheet	12 of 55

INVERTER INTERFACE



LCD CONN



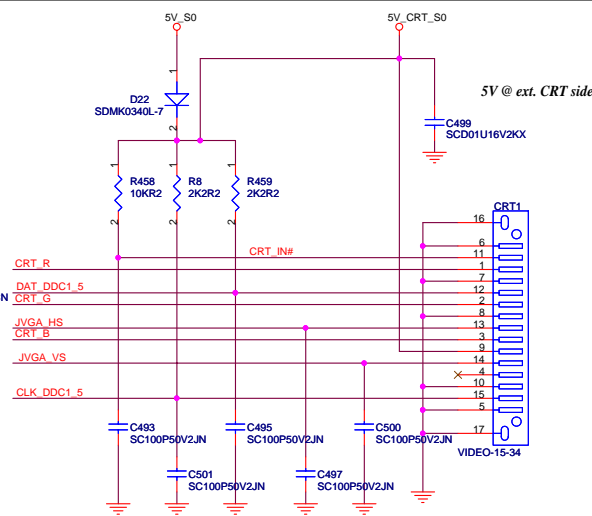
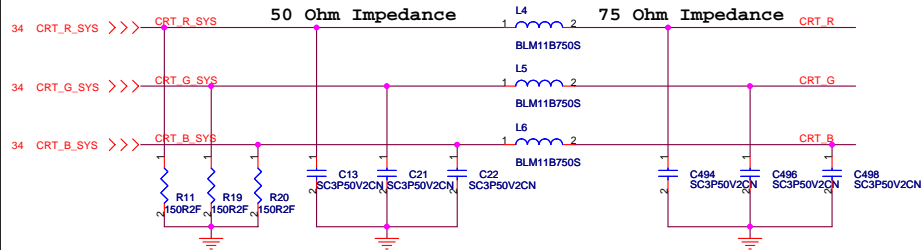
BOM2(NV44+G)

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

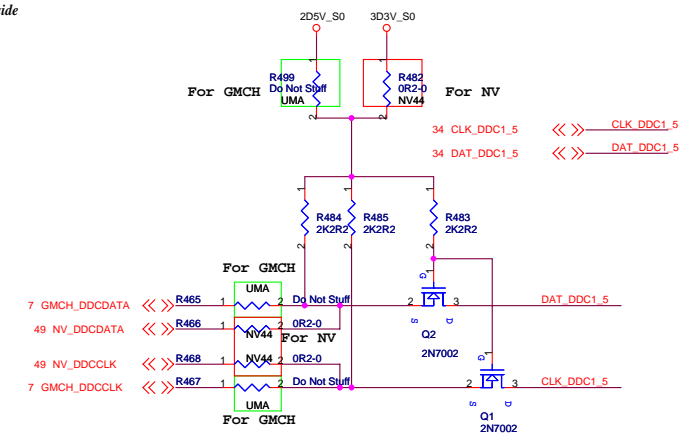
Title			
LCD/Inverter Connector			
Size A3	Document Number		Rev
	CANARY2		SA
Date:	Thursday, January 13, 2005	Sheet 13 of	55

CRT I/F & TV CONNECTOR

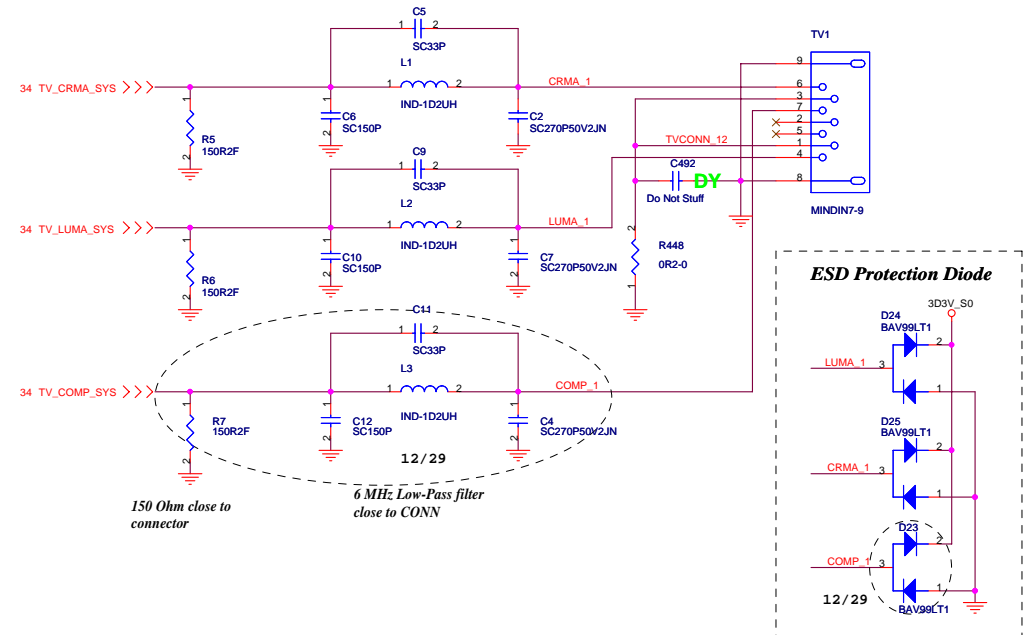
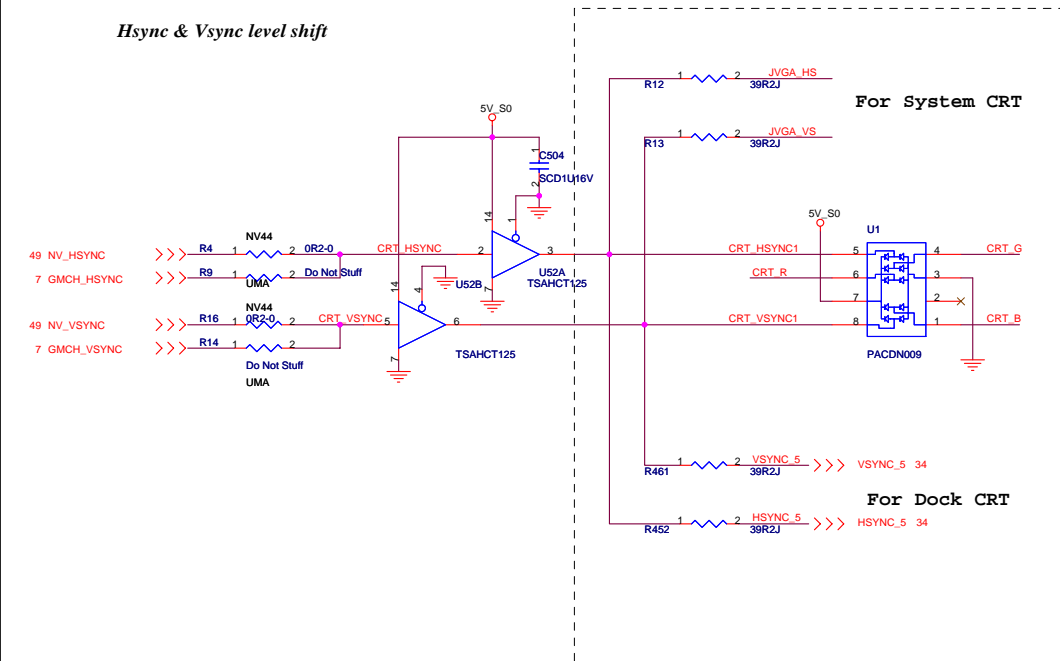
Ferrite bead impedance: 75ohm@100MHz



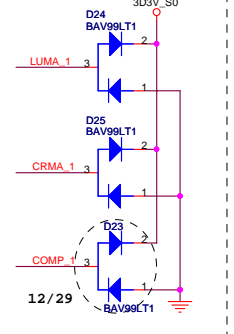
DDC_CLK & DATA level shift



Hsync & Vsync level shift

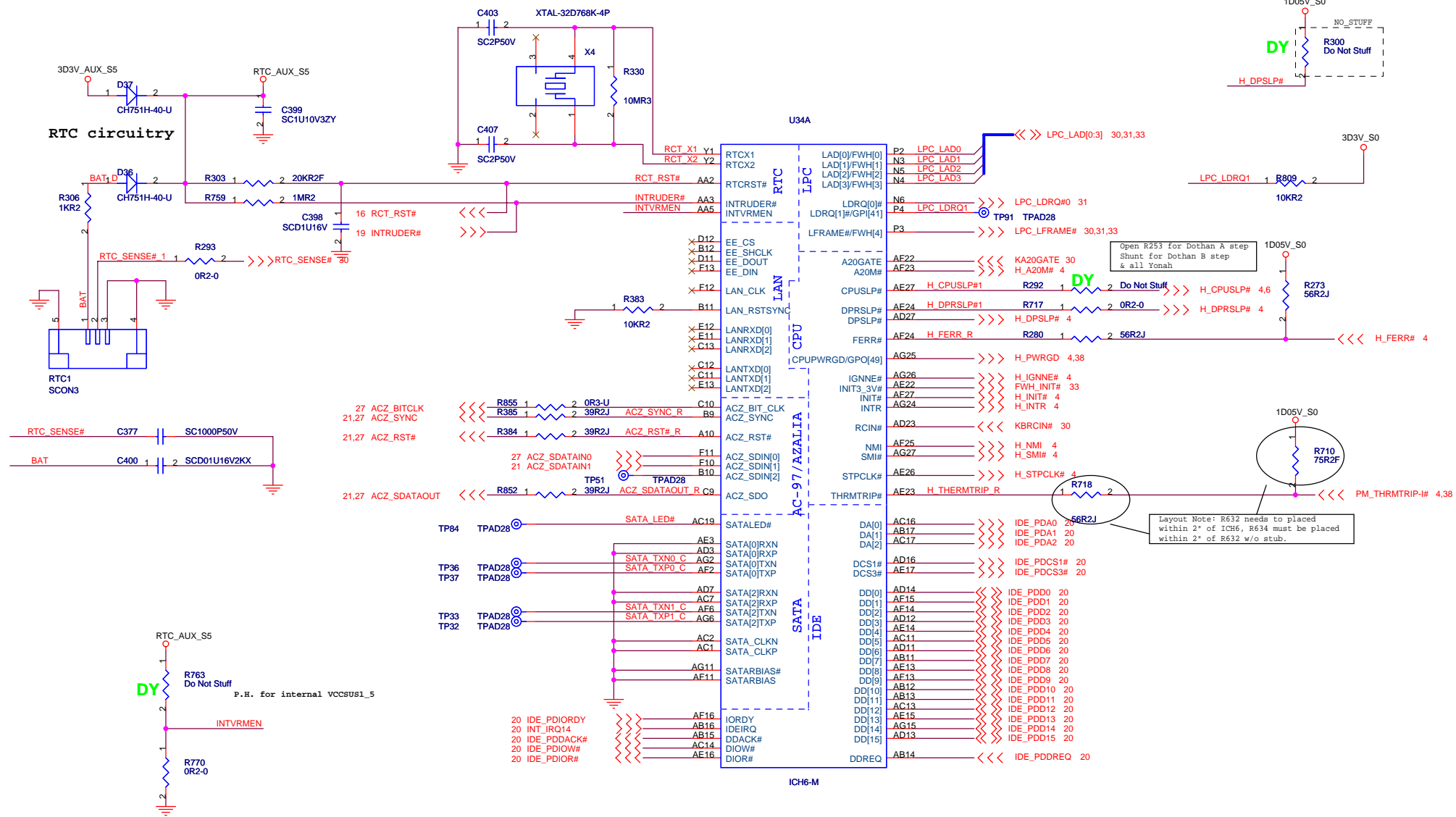


ESD Protection Diode



BOM2(NV44+G)

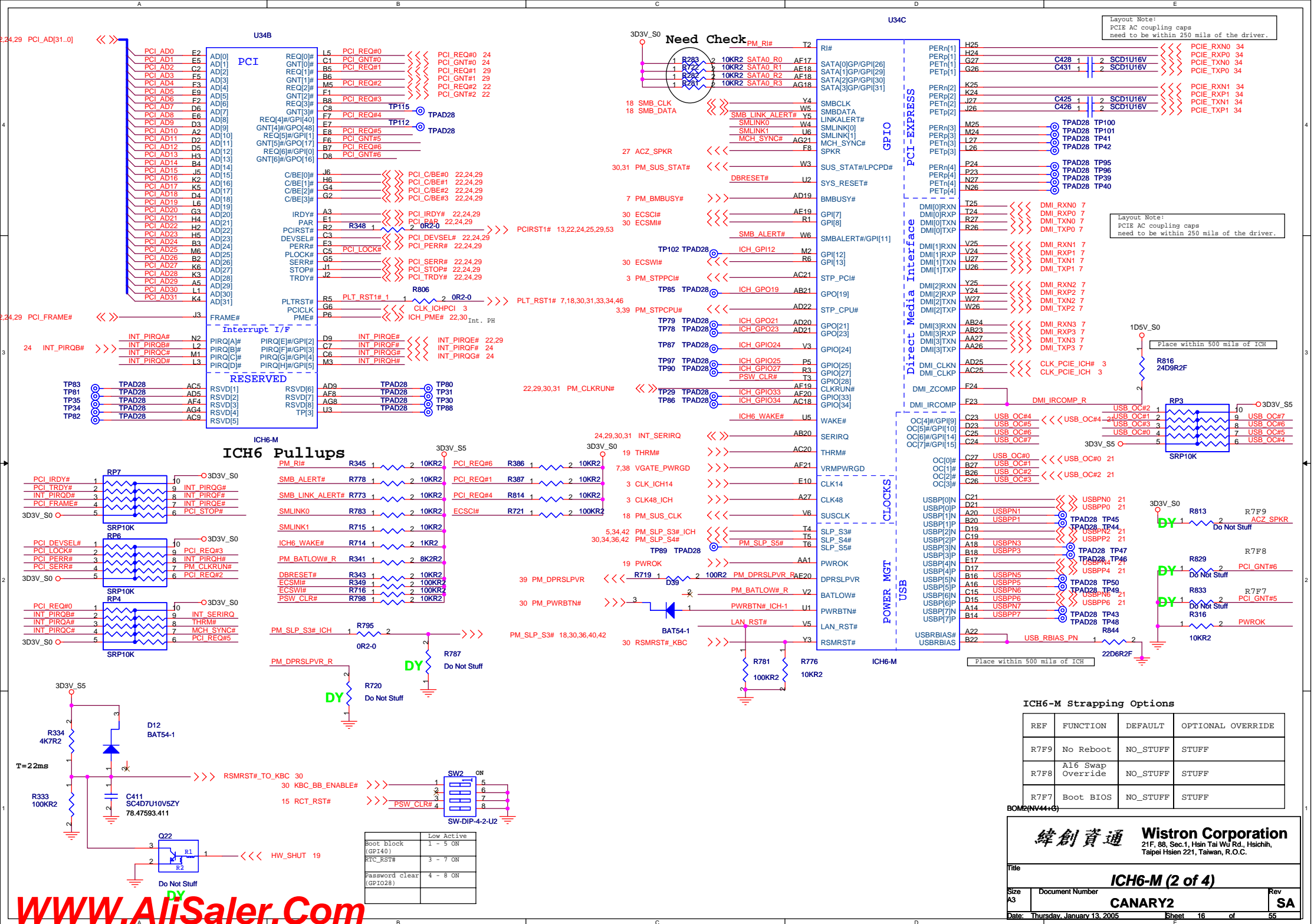
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CRT Connector			
Size	Document Number		Rev
Custom	CANARY2		SA
Date: Thursday, January 13, 2005		Sheet 14 of	55

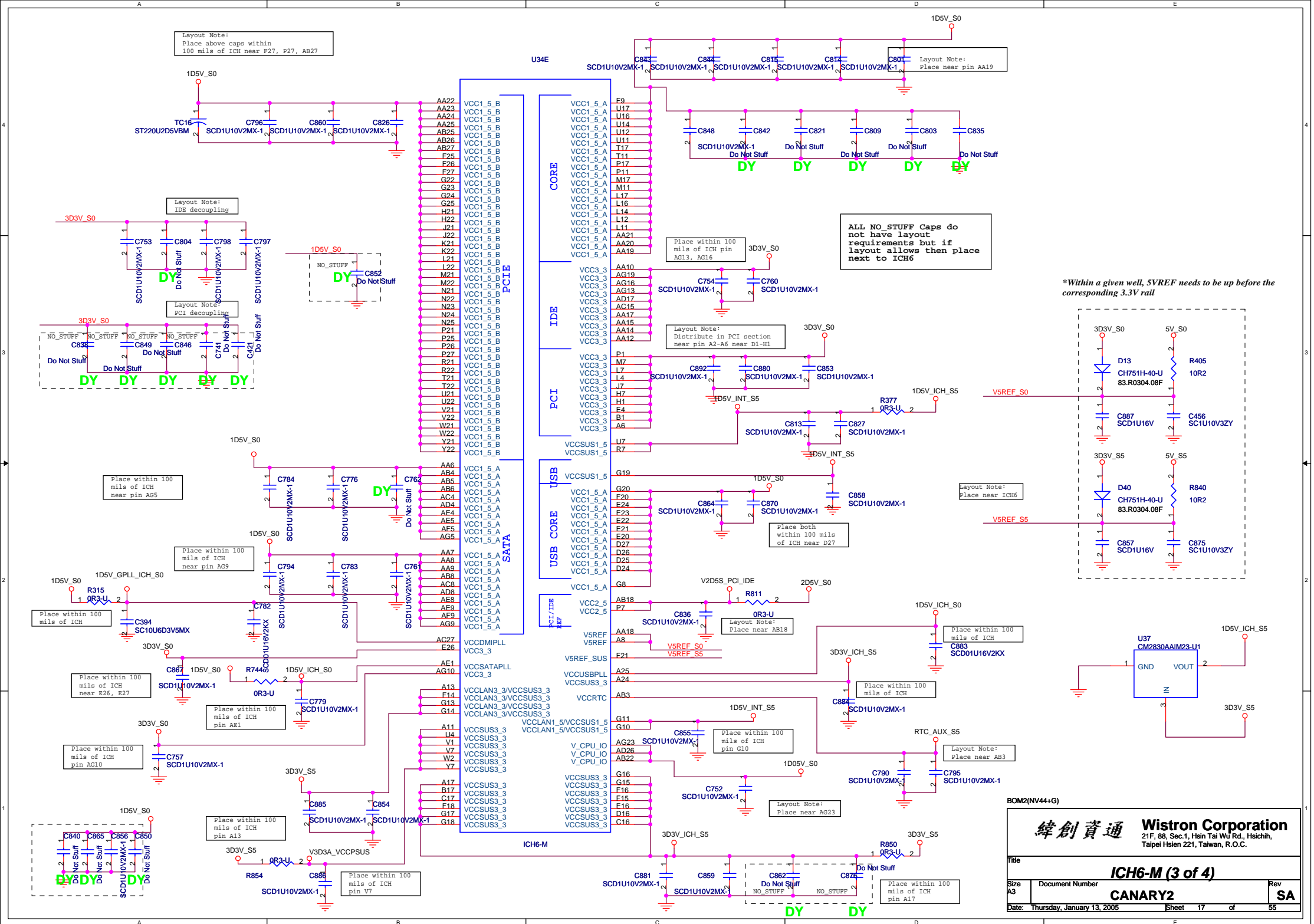


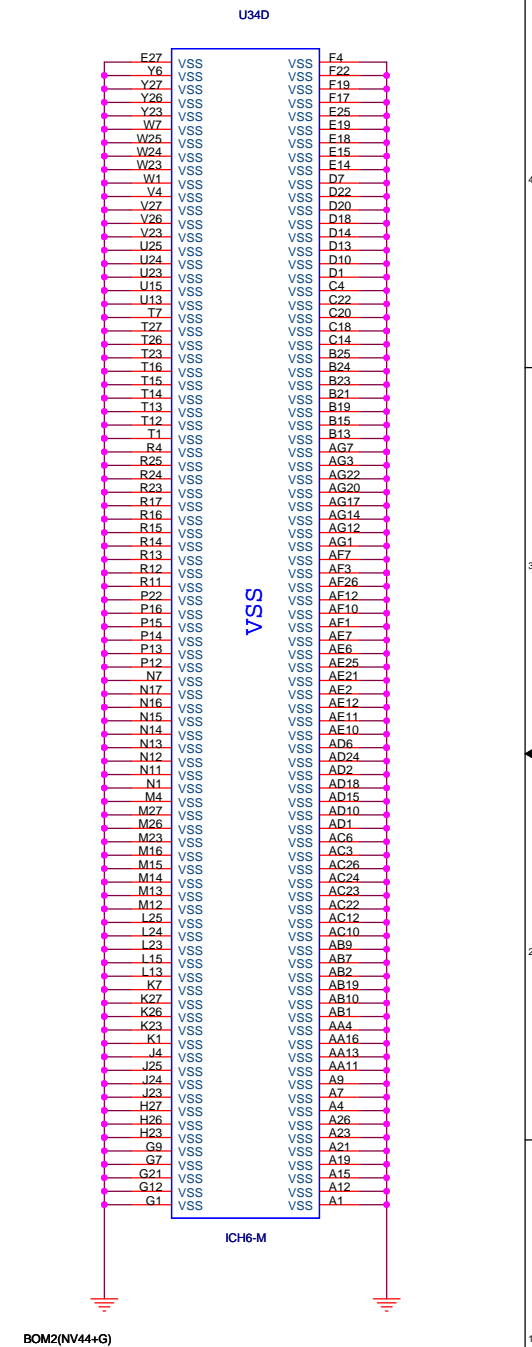
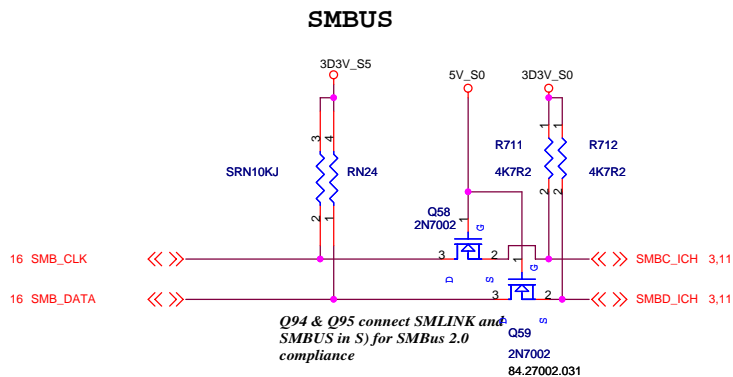
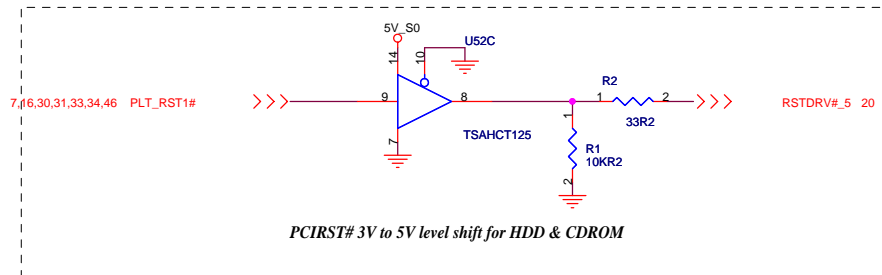
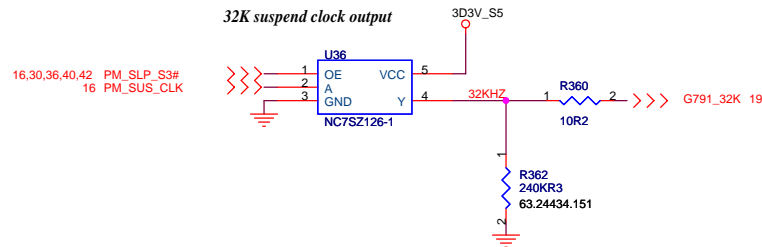
BOM2(NV44+G)

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

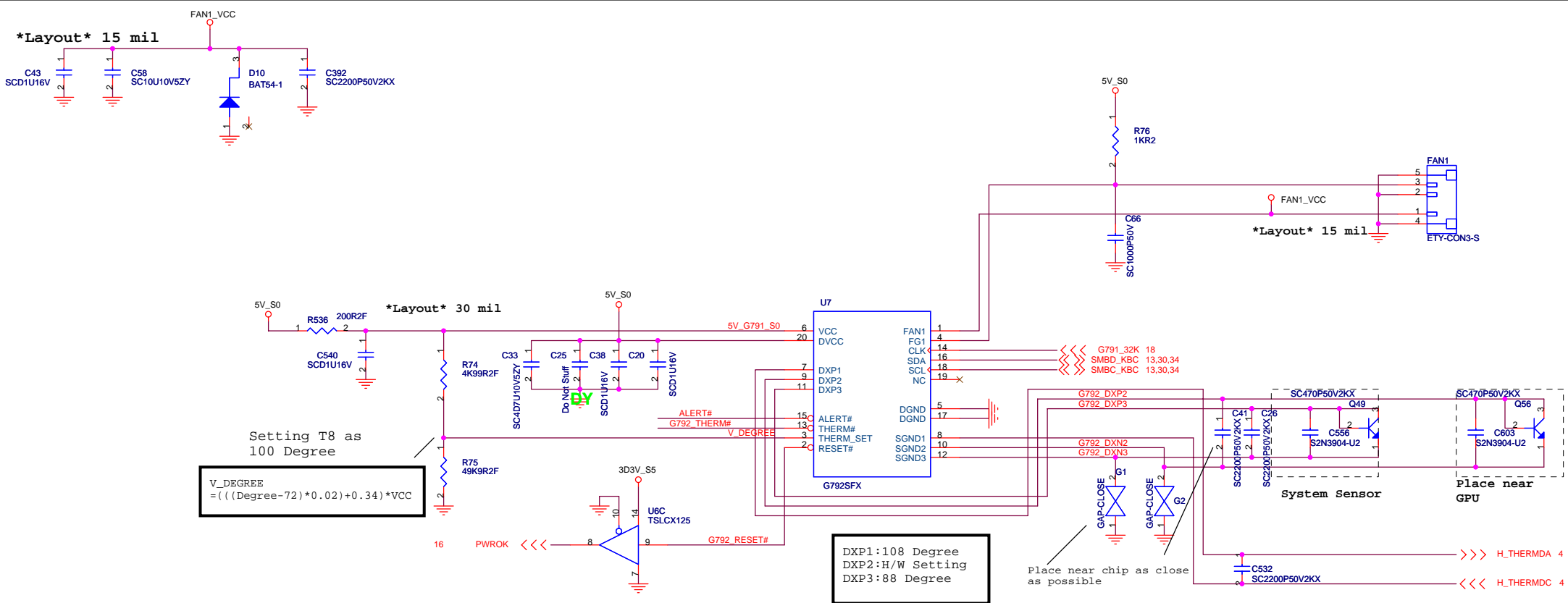
Title ICH6-M (1 of 4)
Size A3 Document Number CANARY2 Rev SA
Date: Thursday, January 13, 2005 Sheet 15 of 55



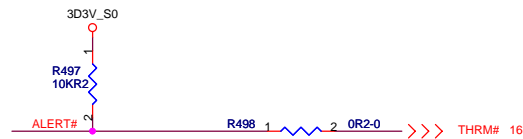




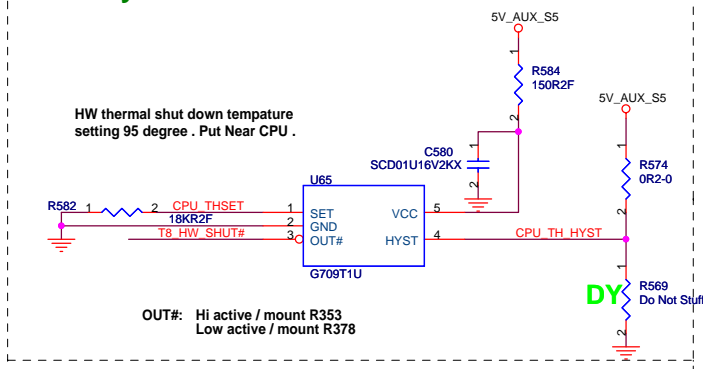
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
ICH6-M (4 of 4)	
Size A3	Document Number CANARY2
Date: Thursday, January 13, 2005	Sheet 18 of 55
Rev SA	



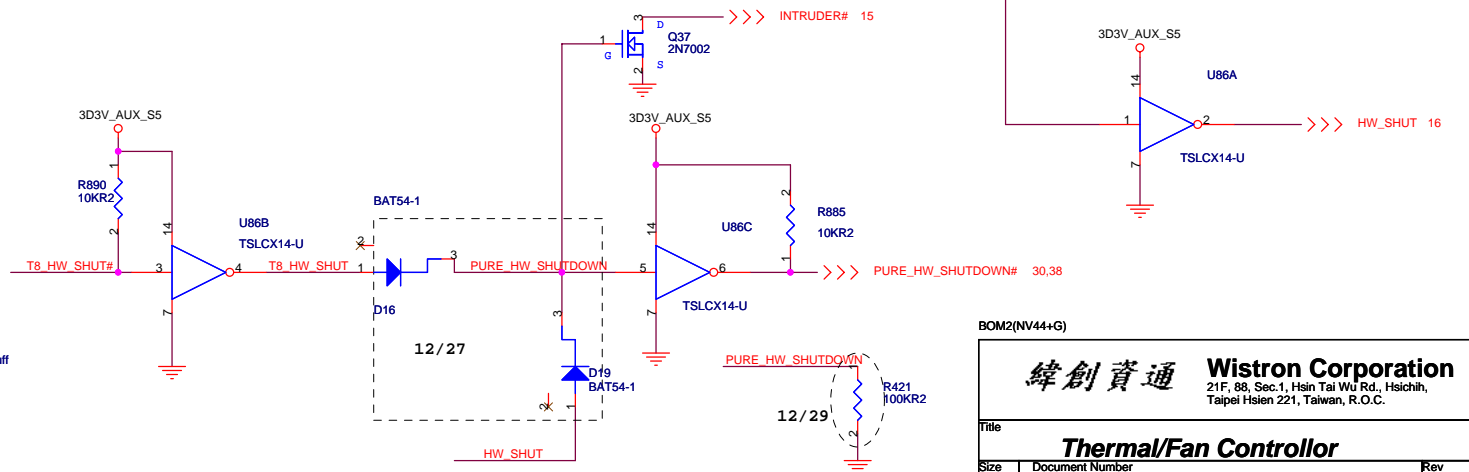
HW thermal shut down temperature setting 95 degree . Put Near CPU .



Dummy when G791 enhanced T8 function



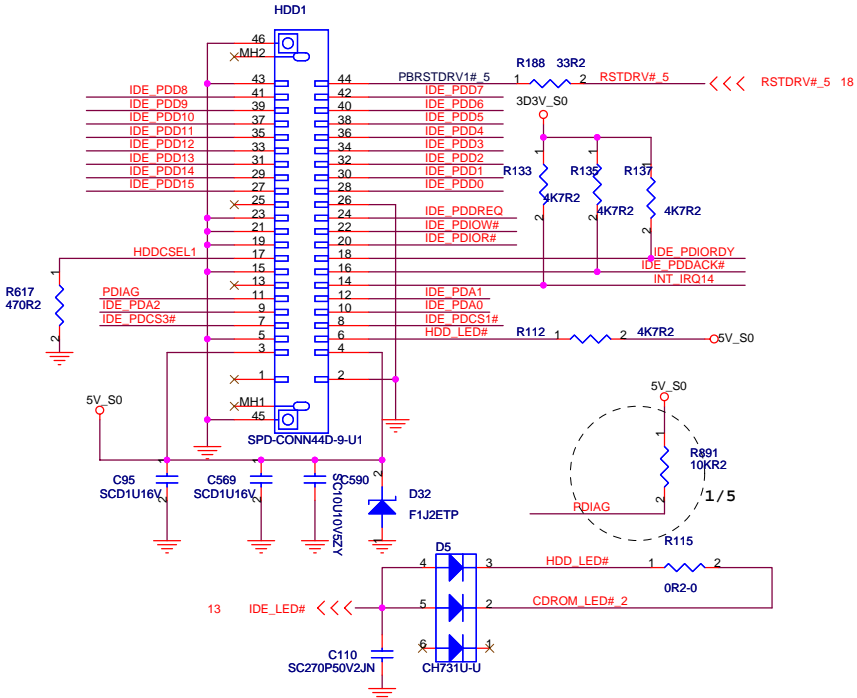
HW Thermal Throttling



BOM2(NV44+G)

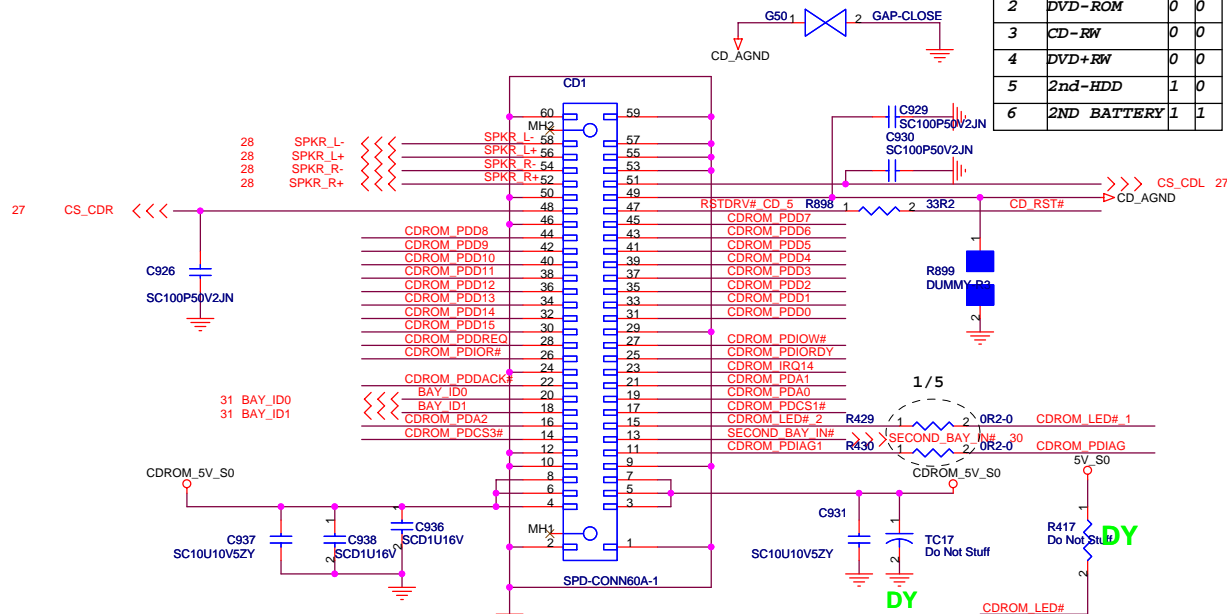
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	Thermal/Fan Controller	
Size Custom	Document Number	Rev
	CANARY2	SA
Date: Thursday, January 13, 2005	Sheet 19 of	55

HDD Connector



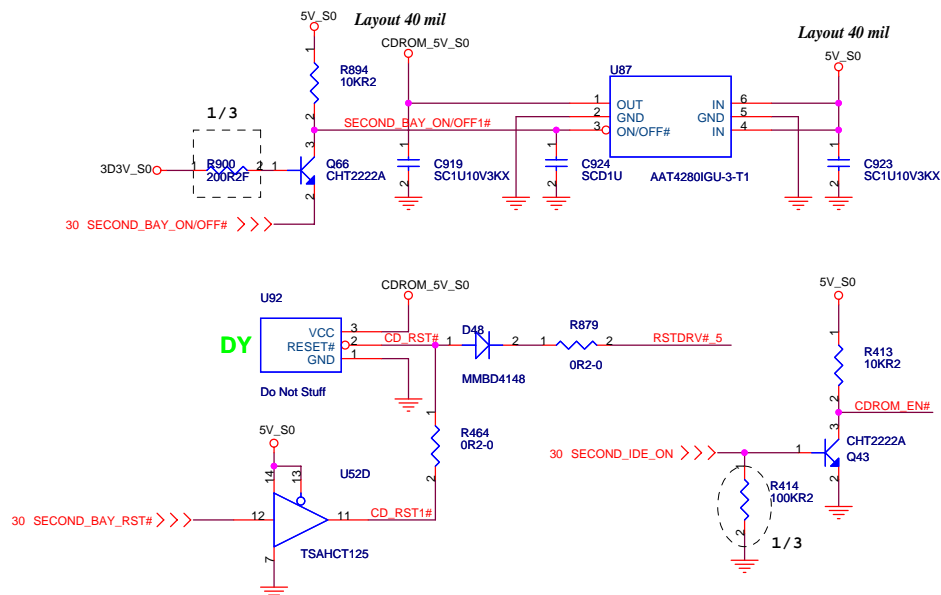
CD-ROM Connector

BAY Option Table			
Type	Device Description	BAY0	BAY1
1	CD-ROM	0	0
2	DVD-ROM	0	0
3	CD-RW	0	0
4	DVD+RW	0	0
5	2nd-HDD	1	0
6	2ND BATTERY	1	1

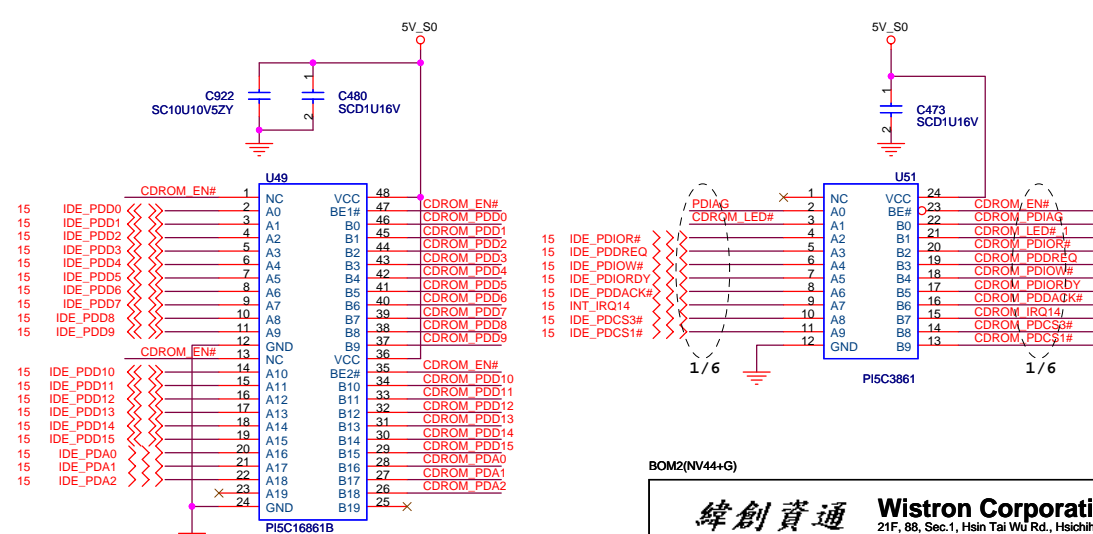


CHECK PIDE/SIDE DIAG# PIN

HOT SWAP CIRCUIT



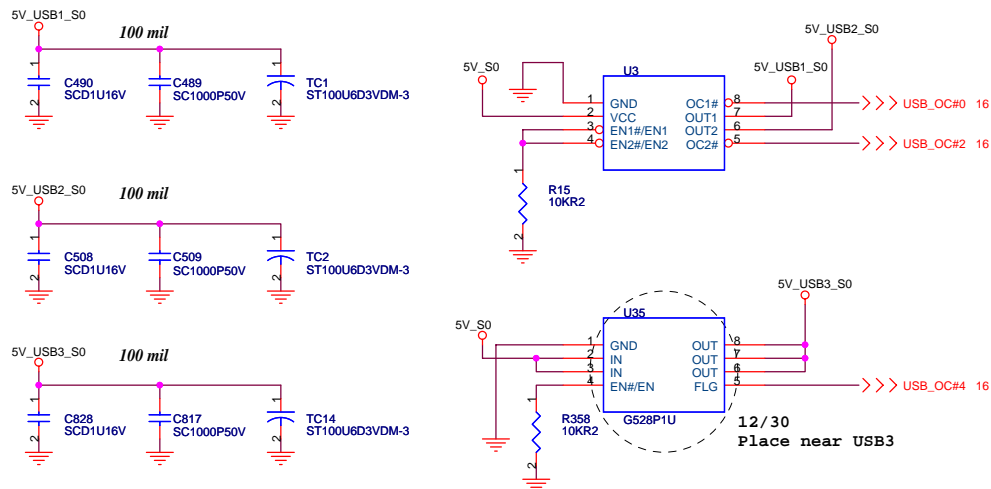
TRI-STATE SWITCH FOR CDROM HOT SWAP



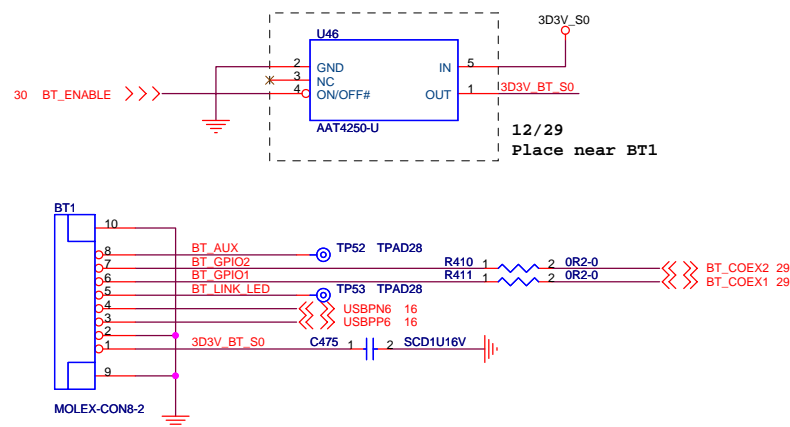
BOM2(NV44+G)

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

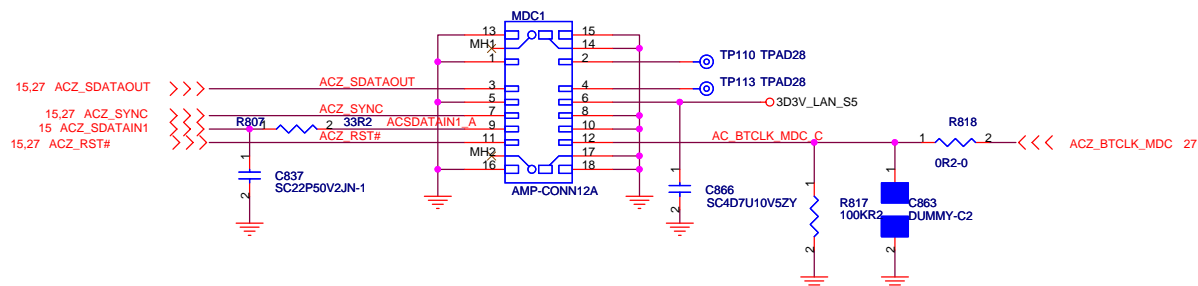
Title			
HDD and CDROM			
Size A3	Document Number		Rev
	CANARY2		S
Date: Thursday, January 13, 2005	Sheet 20	of	55



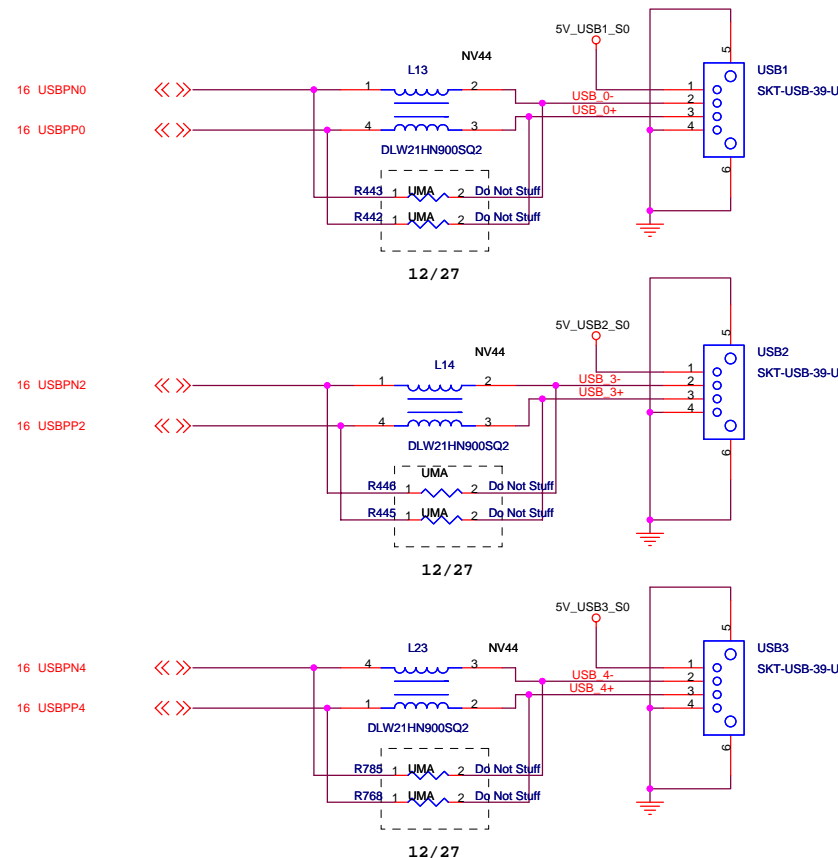
BLUETOOTH MODULE CONNECTOR



MDC 1.5 CONNECTOR



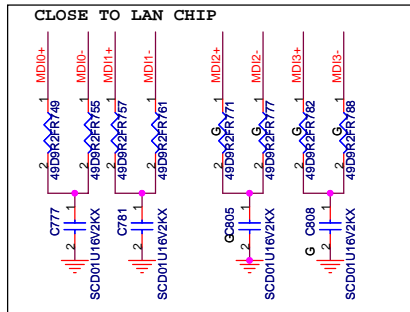
USB PORT



BOM2(NV44+G)

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title			
USB & MDC & BTOOTH			
Size	Document Number	Rev	
A3	CANARY2	SA	
Date:	Thursday, January 13, 2005	Sheet	21 of 55

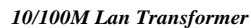


```

===== >>> 100M_LED# 23,34
===== >>> 10M_LED# 23
===== >>> LAN_ACT_LED# 23
===== >>> 1G_LED# 23

```

BOM2(NV44+G)			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN RTL8110SBL			
Size A3	Document Number	CANARY2	Rev SA
Date:	Thursday, January 13, 2005	Sheet	22 of 55



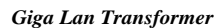
Function	SEL
An to nB1	L
An to nB2	H

```

Green LED: Speed 100: ON / Speed 10:OFF
Yellow LED: Link: ON, TX/RX:
Flash(10Hz) -----

```

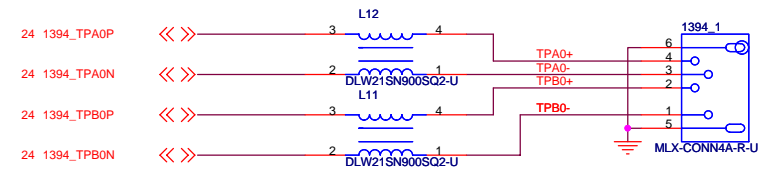
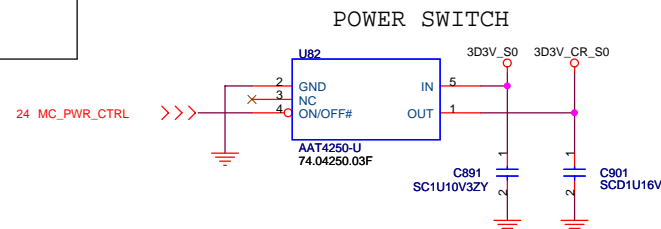
DOC_TIP, DOC_RING, TIP, RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



BOM2(NV44+G)

LAN Connector			
Document Number	CANARY2		Rev SA
Date: Thursday, January 13, 2005	Sheet 23	of	55

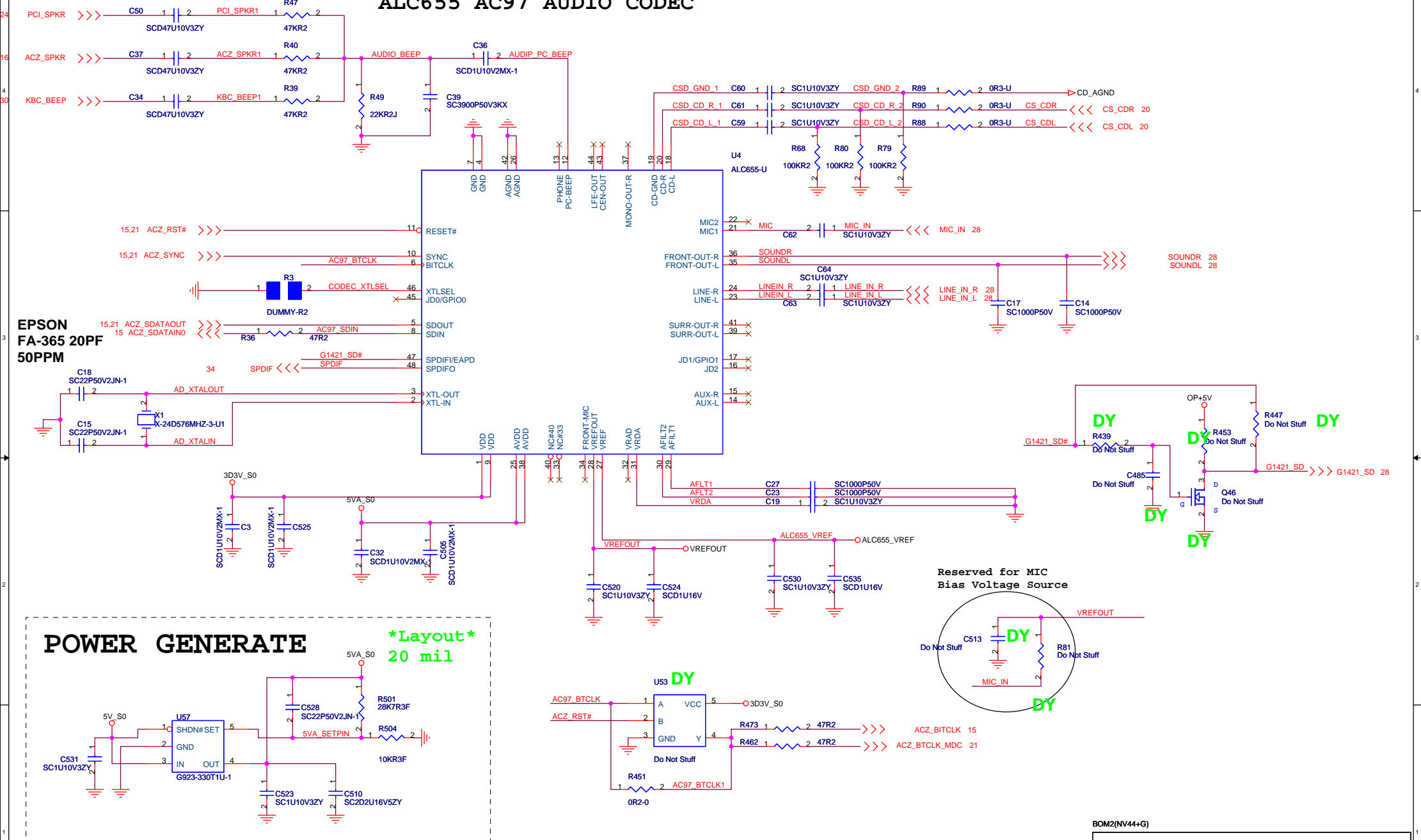
WWW.AliSaler.Com

[illegible]

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCMCIA SLOT / 1394 CONN.			
Size A3	Document Number		Rev
	CANARY2		SA
Date: Thursday, January 13, 2005	Sheet	26 of	55

ALC655 AC97 AUDIO CODEC



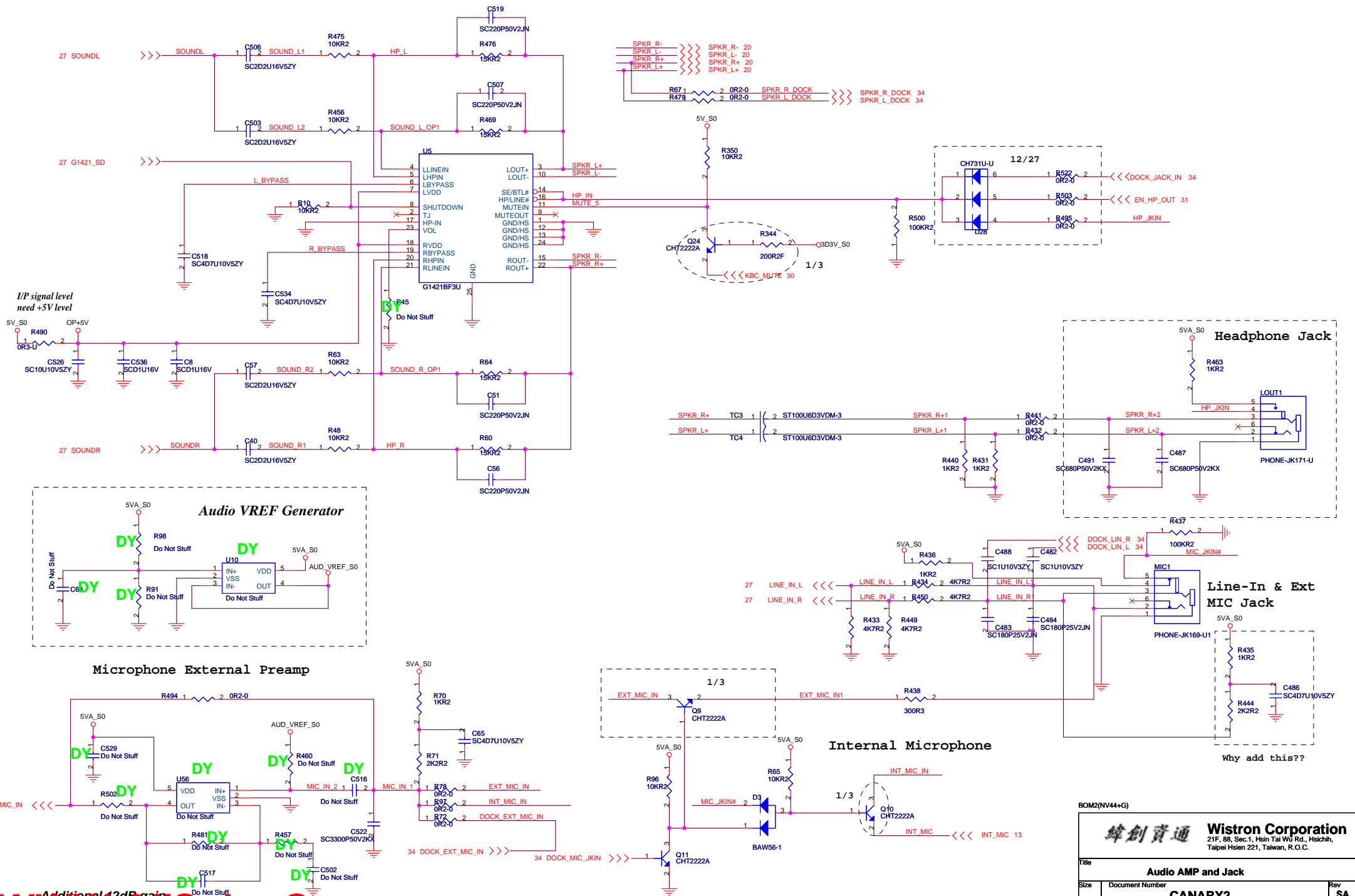
BOM2(NV44+G)

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
AC'97 CODEC - ALC655			
Size A3	Document Number		Rev
	CANARY2		SA
Date:	Thursday, January 13, 2005	Sheet 27 of	55

AUDIO OP AMPLIFIER



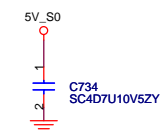
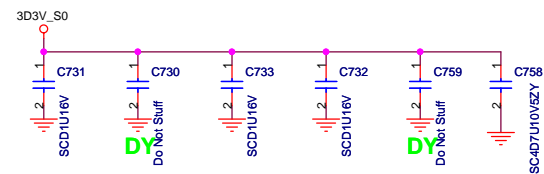
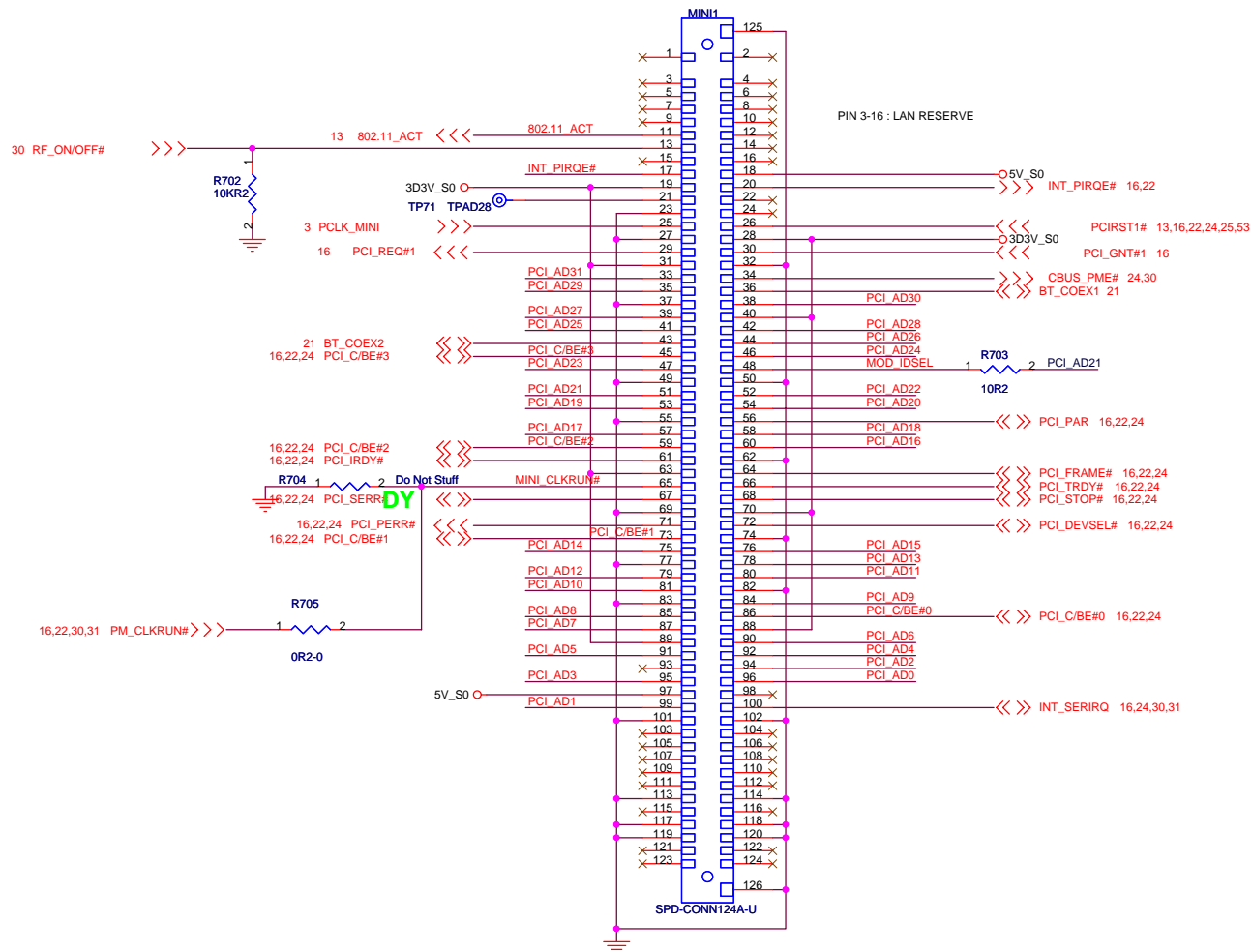
BOM2(NV44+G)

緯創資通

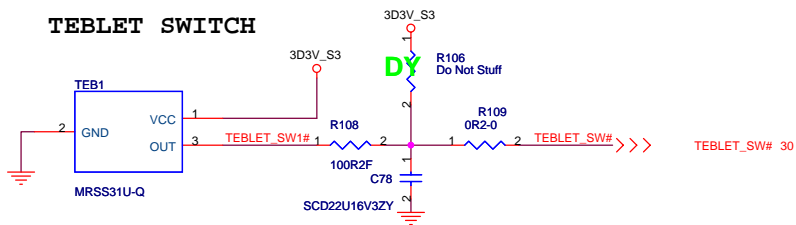
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Audio AMP and Jack			
Size	Document Number		Rev
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Date:	Thursday, January 13, 2005	Sheet 28 of	55

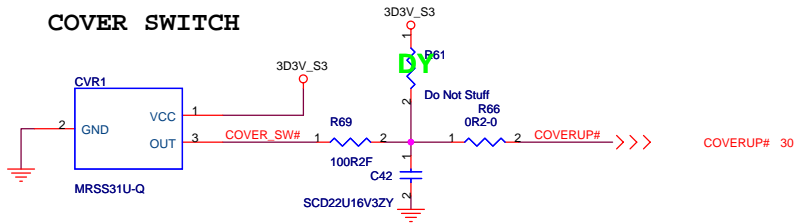
Additional 12dB gain



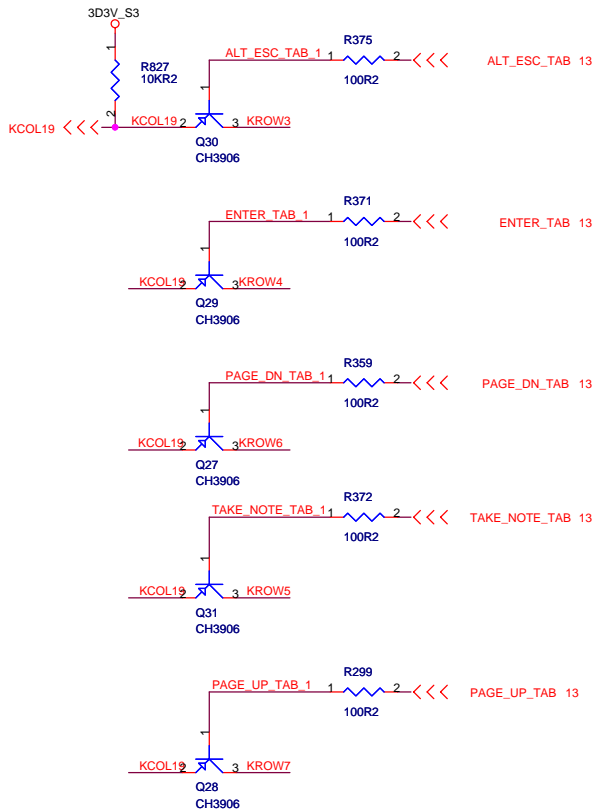
TEBLET SWITCH



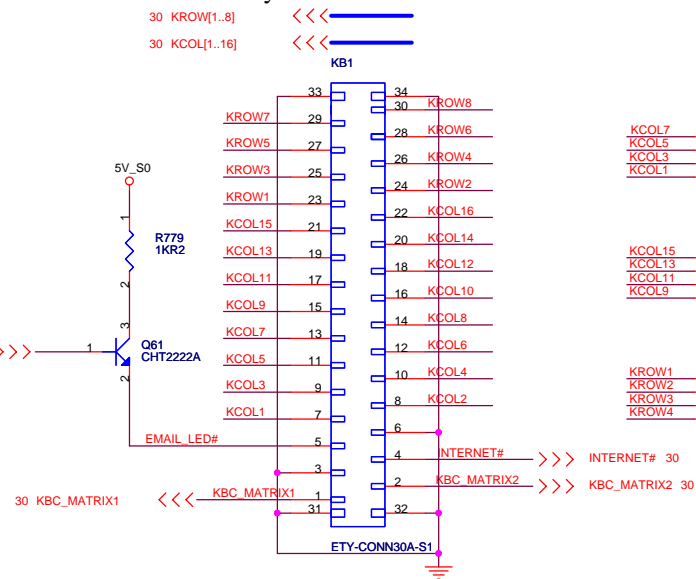
COVER SWITCH



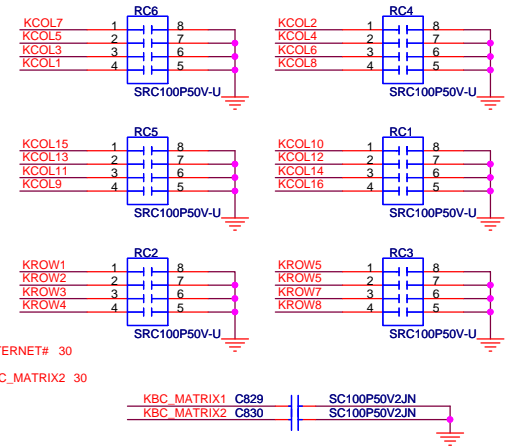
TABLET FUNCTION BUTTON



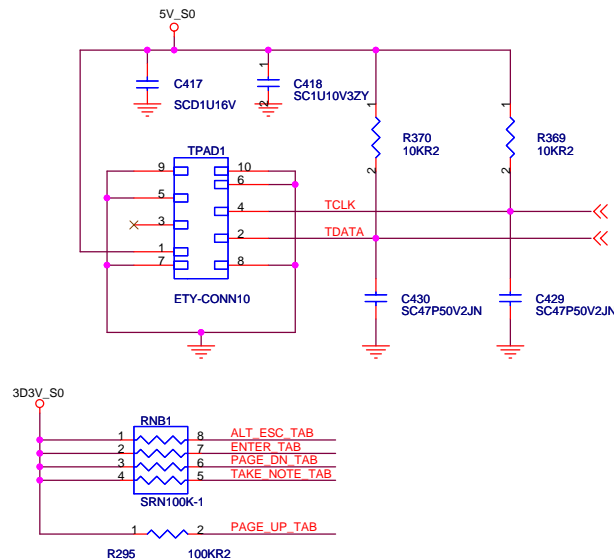
Internal Keyboard Connector



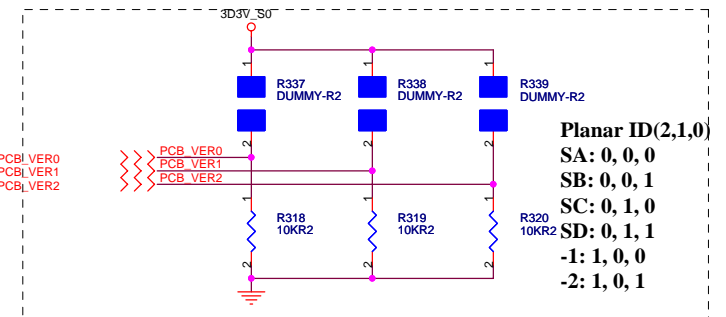
EMI CAPS



TouchPad Connector



Board ID

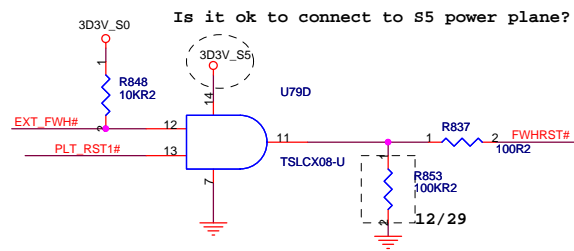


Keyboard matrix

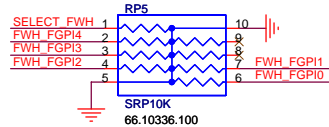
	US	Jap	Europe	US international
MATRIX1	HIGH	LOW	HIGH	HIGH
MATRIX2	HIGH	HIGH	LOW	HIGH

BOM2(NV44+G)

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Title			
KBC&TPAD CONN			
Size A3	Document Number	Rev	
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Date: Thursday, January 13, 2005	Sheet 32	of	55



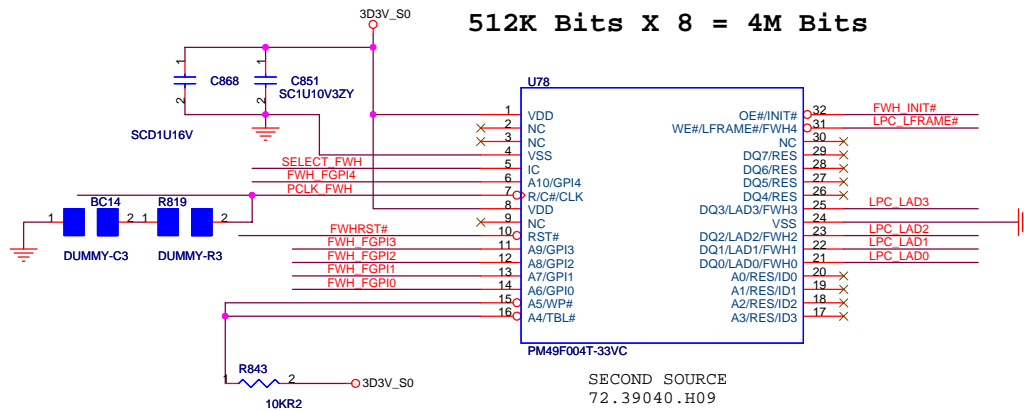
Unused FGPI pins must not be float



15,30,31 LPC_LAD[0:3] << >>

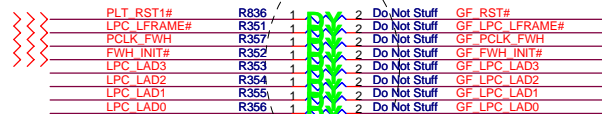
FLASH ROM

512K Bits X 8 = 4M Bits



SECOND SOURCE
72.39040.H09

7,16,18,30,31,34,46 PLT_RST1#
15,30,31 LPC_LFRAME#
3 PCLK_FWH
15 FWH_INIT#



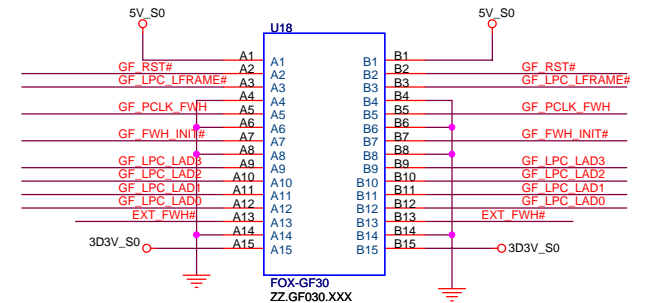
12/30

TOP VIEW

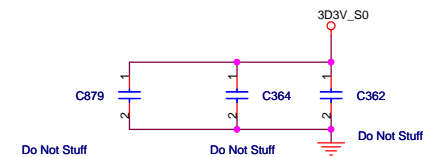
A15 (B1)
A14 (B2)
:
:
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

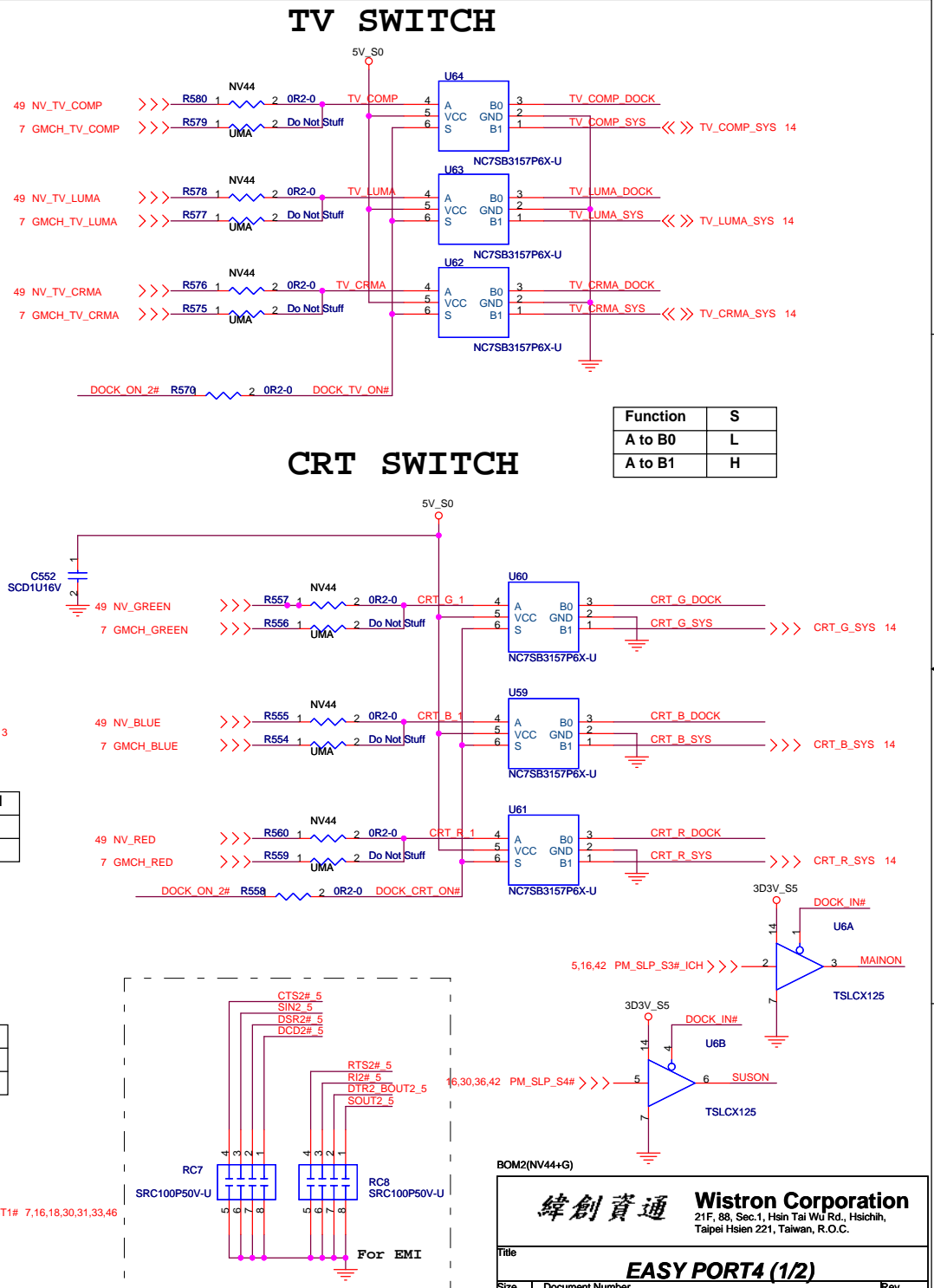
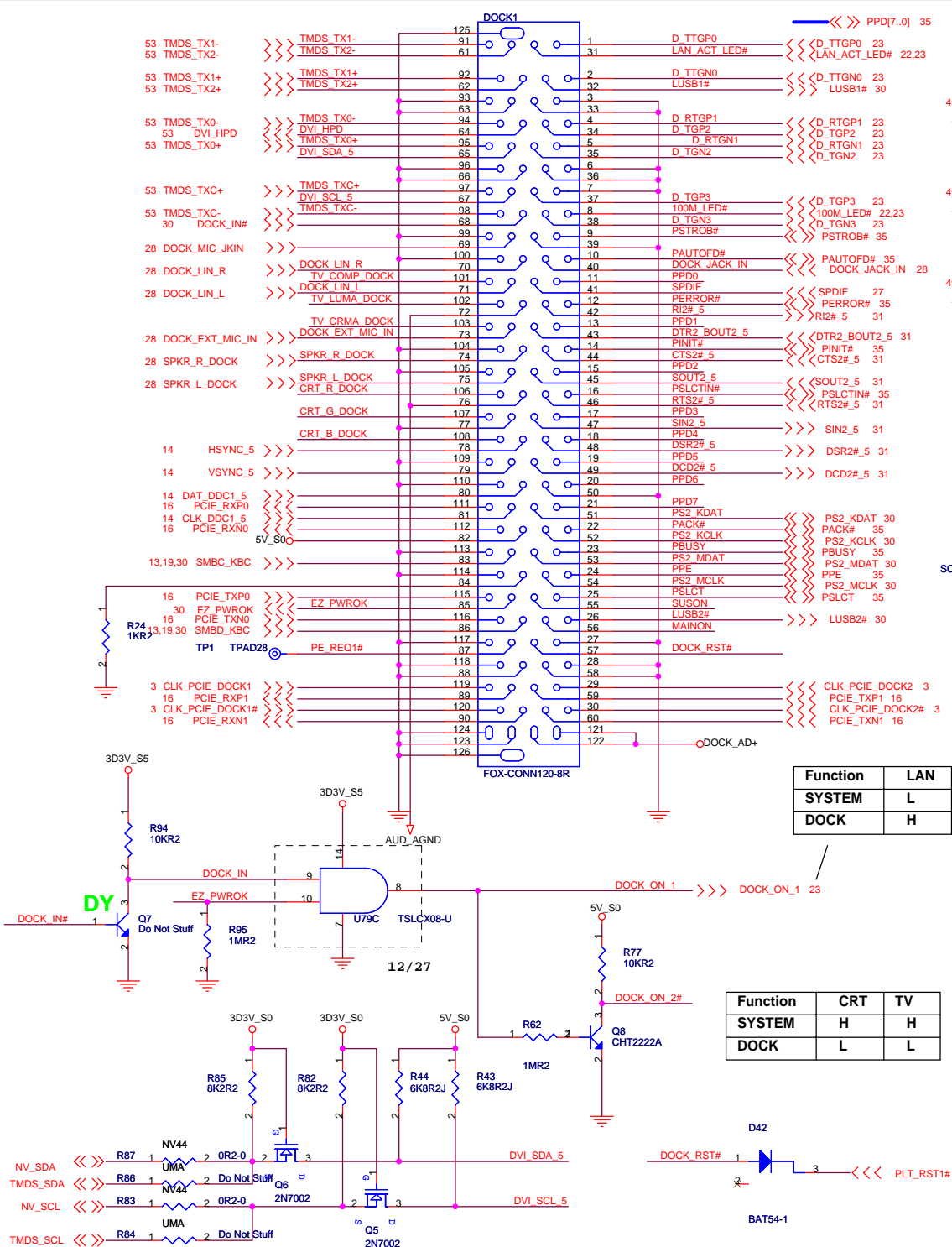


DY DY DY

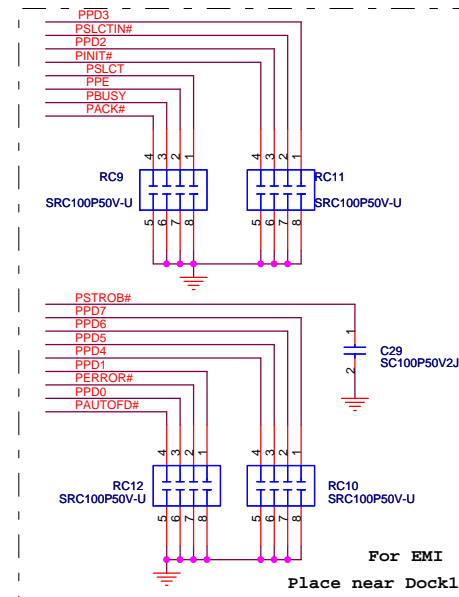
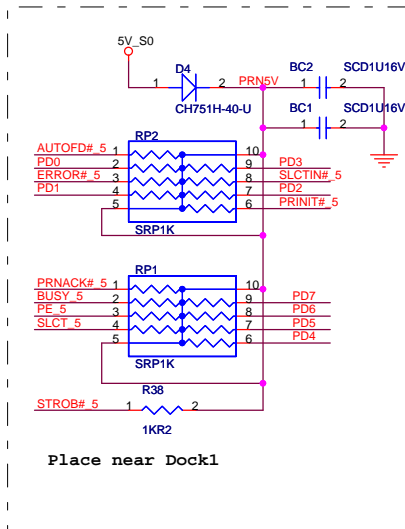
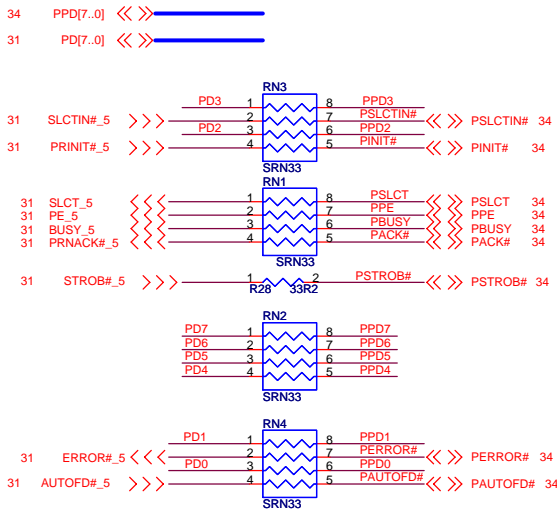
BOM2(NV44+G)

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

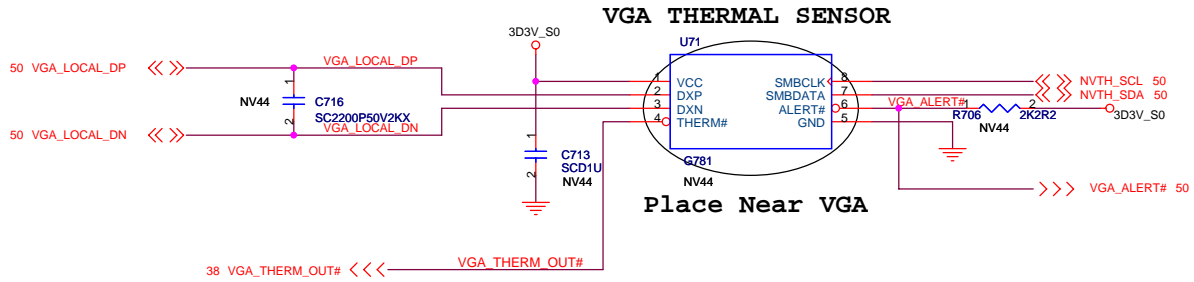
Title
FWH and Debug
Size A3 Document Number
CANARY2
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Rev SA



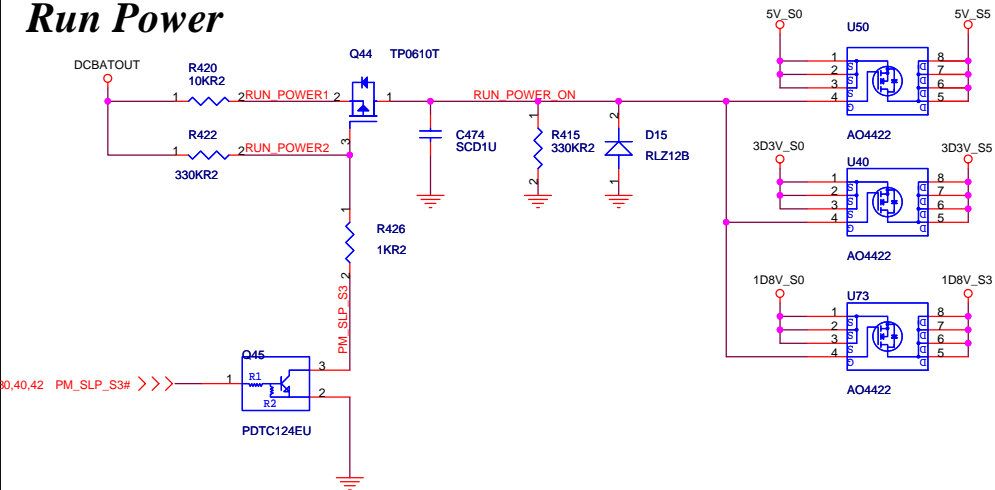
PRINT PORT



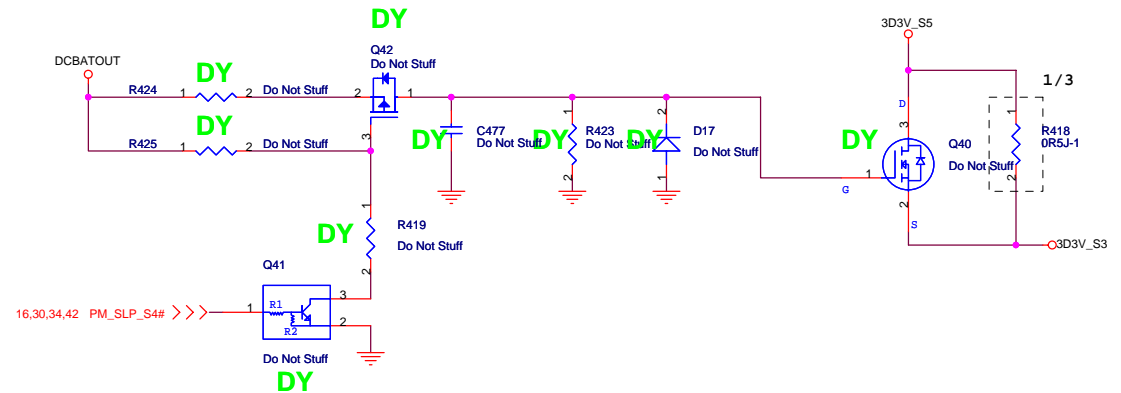
I2C ADDRESS: 0x98H



Run Power



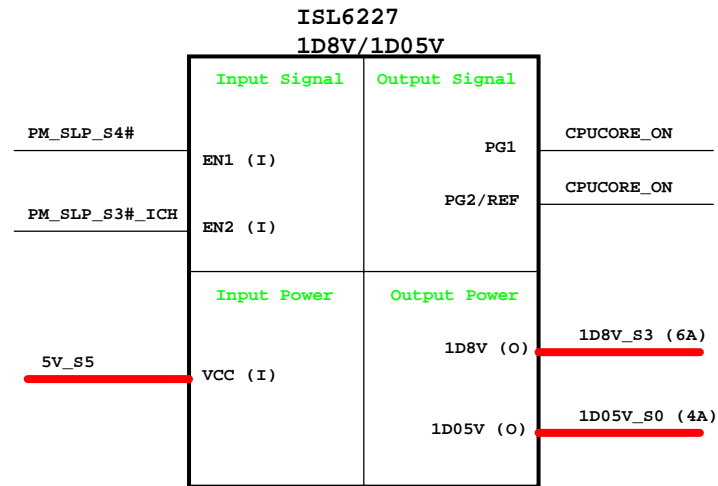
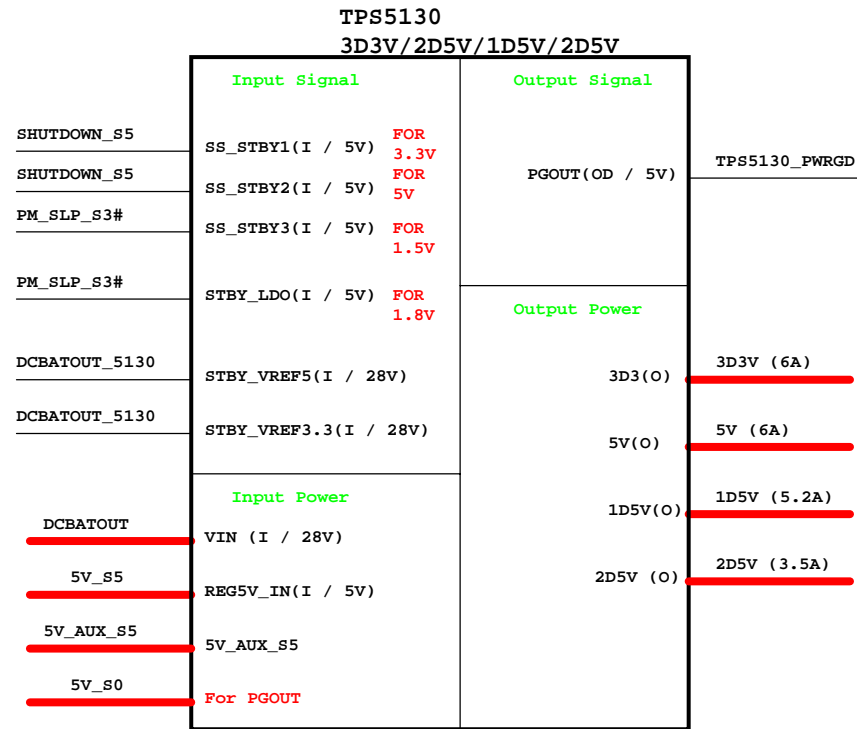
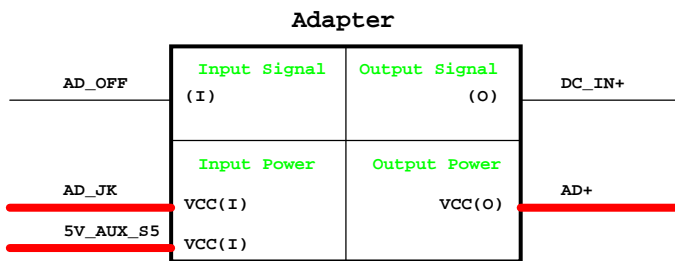
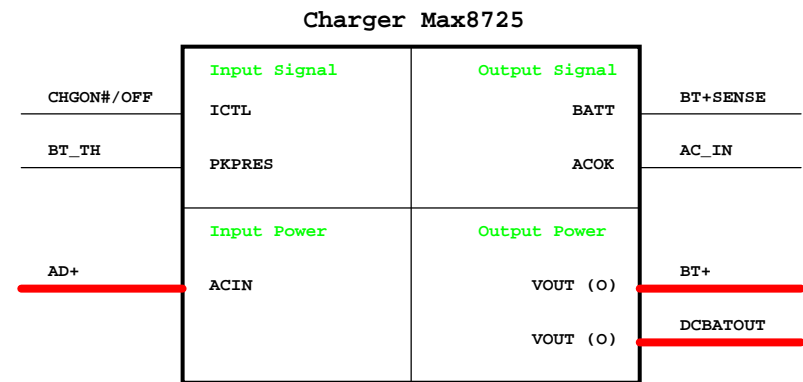
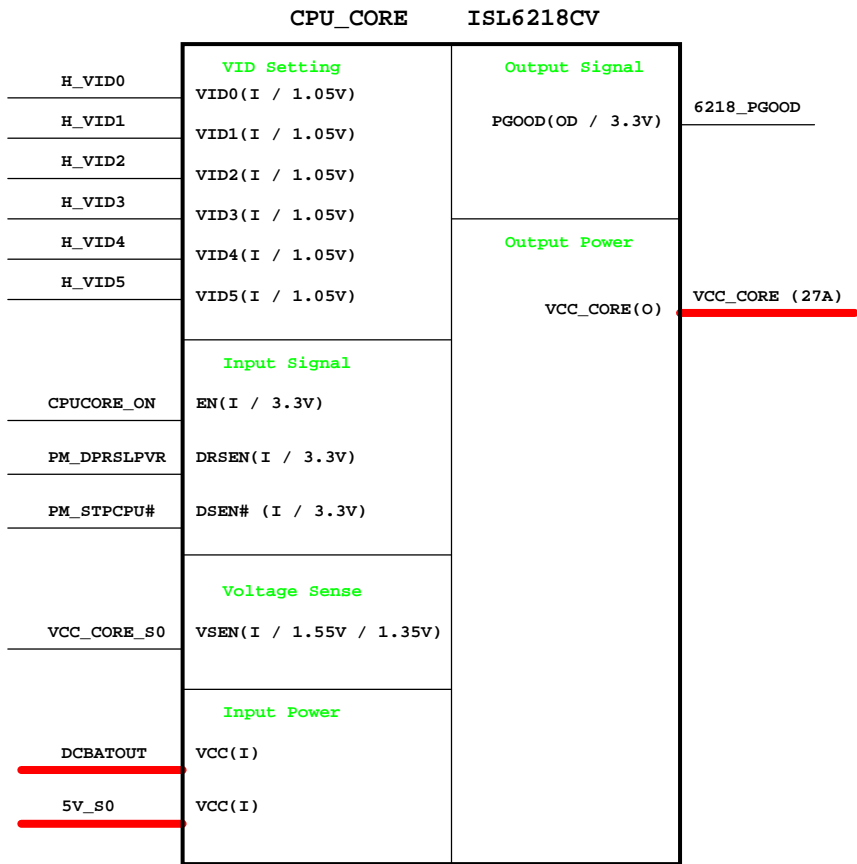
Suspend Power



BOM2(NV44+G)

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Taipei Hsien 221, Taiwan, R.O.C.

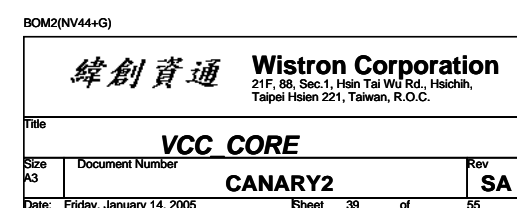
Title			
<i>RUN and SUSPEND Power</i>			
Size A3	Document Number CANARY2		Rev SA
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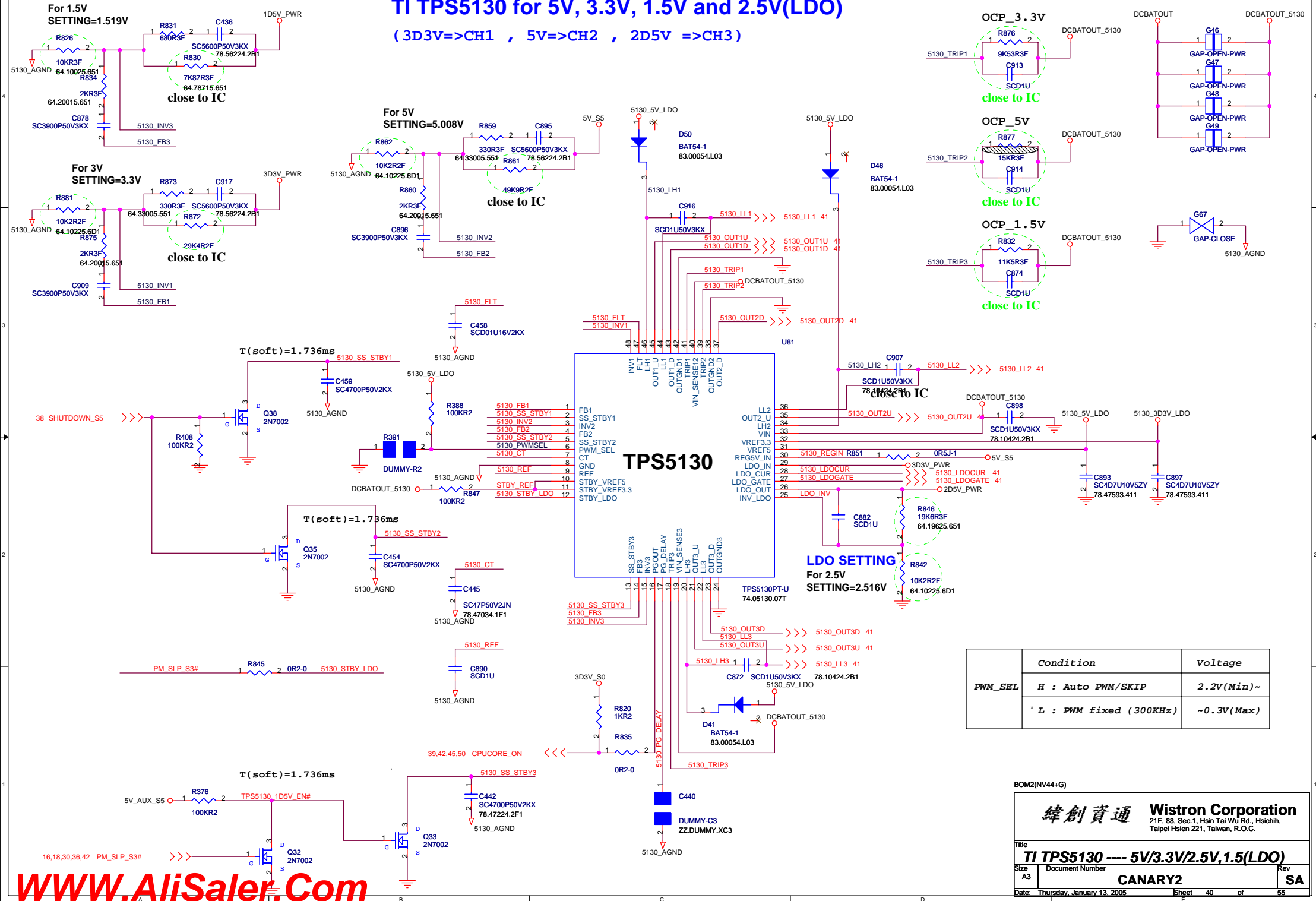
POWER BUTTON

Title			
POWER ON CIRCUIT			
Size A3	Document Number		Rev
	CANARY2		SA
Date: Thursday, January 13, 2005	Sheet 38	of	55

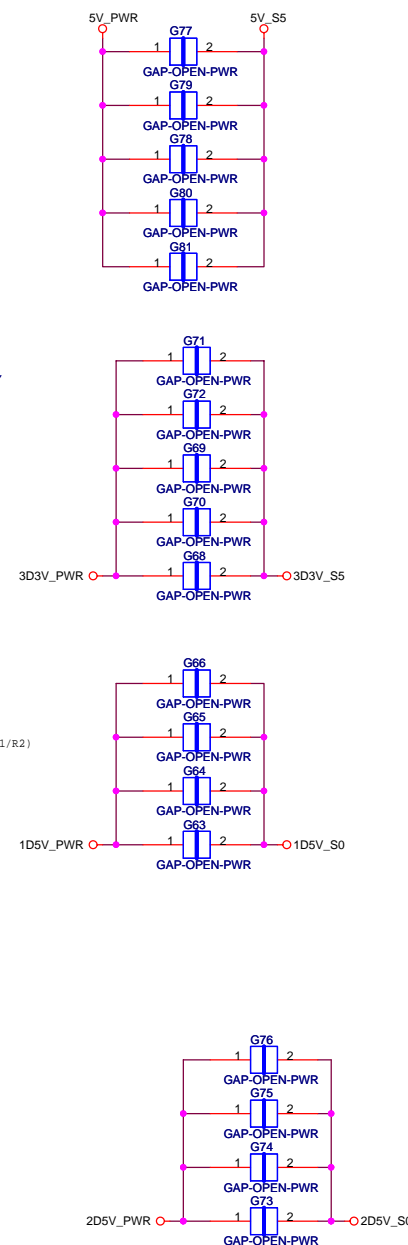
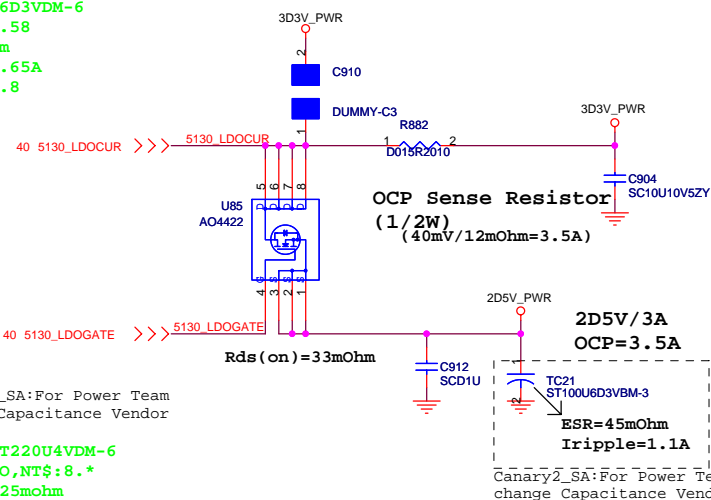
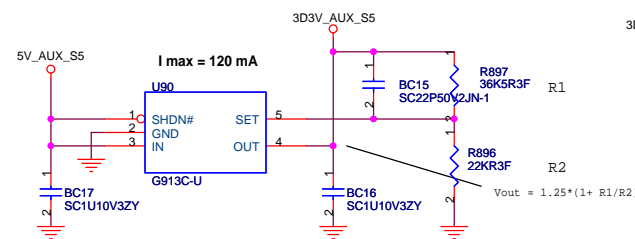
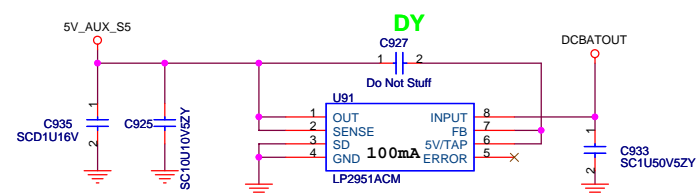


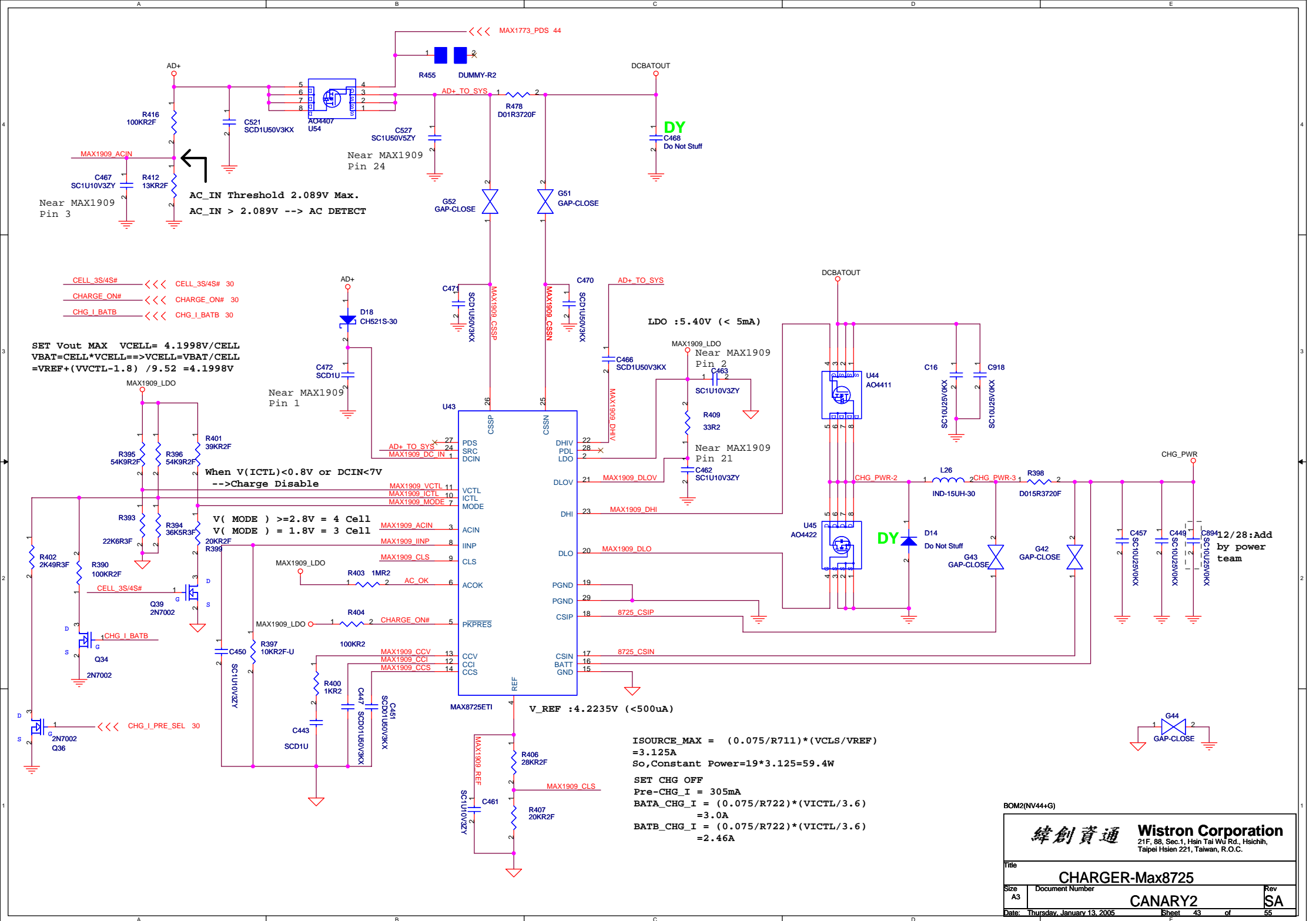
TI TPS5130 for 5V, 3.3V, 1.5V and 2.5V(LDO)

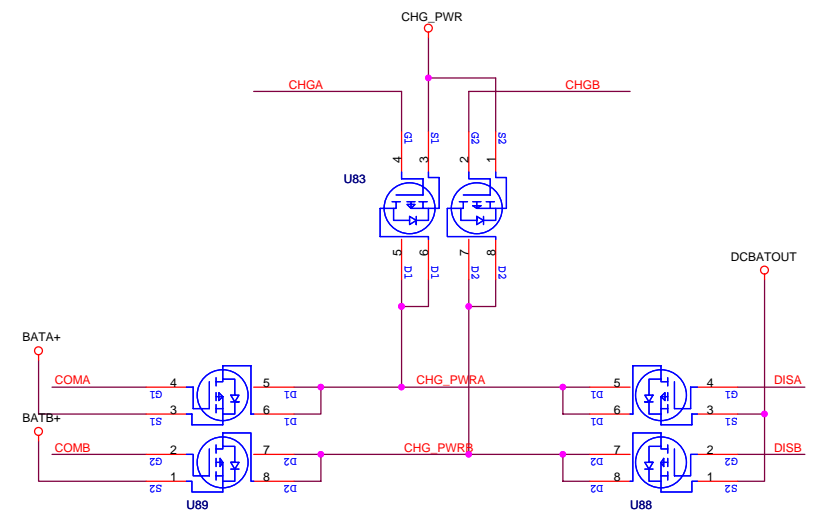
(3D3V=>CH1 , 5V=>CH2 , 2D5V =>CH3)



(3D3V=>CH1 , 5V=>CH2 , 2D5V =>CH3)





[illegible]

CONNECTOR

5V_AUX_S5

CONNECTOR

D21
Do Not Stuff
Do Not Stuff

D20
Do Not Stuff
Do Not Stuff

DY

R427 27R2J

R428 27R2J

BATA+ 1

30 BATA_SCL 2

30 BATA_SDA 3

30 BATA_IN# 4

BATA_CLK 1

BATA_DAT 1

C478 SCD1U

C481 SC1000P50V

C479 DUMMY-C3

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SYN-CON7-S-U

BAT+ 1

2

3

4

5

6

7

[illegible]

Adaptor IN Detection

BOM2(NV44+G)

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD&BTY CONNECTER & BTY SWITCH**

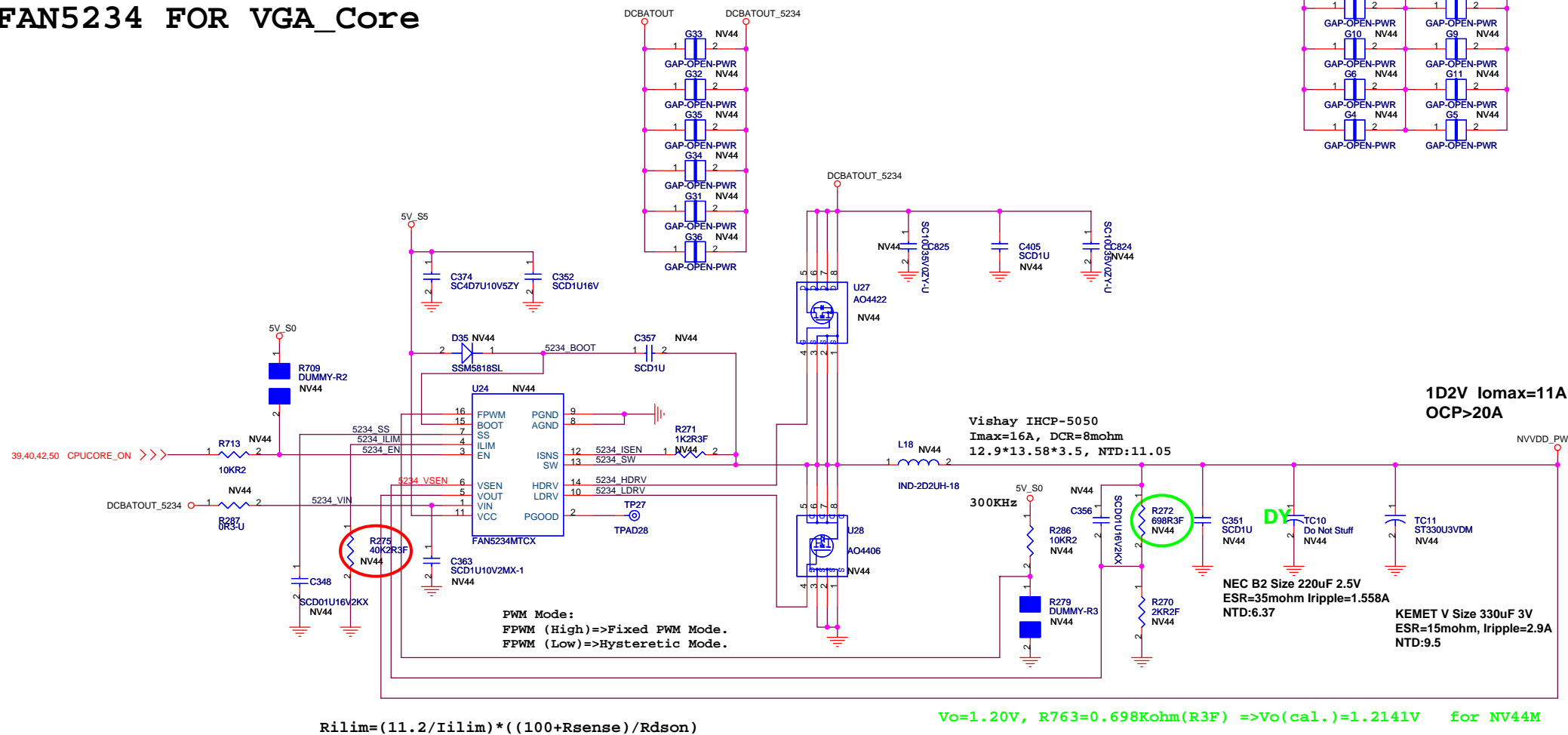
Size A3 Document Number: **CANARY2**

12/29

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
AD&BTY CONNECTER & BTY SWITCH			
Size	Document Number		Rev
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FAN5234 FOR VGA Core



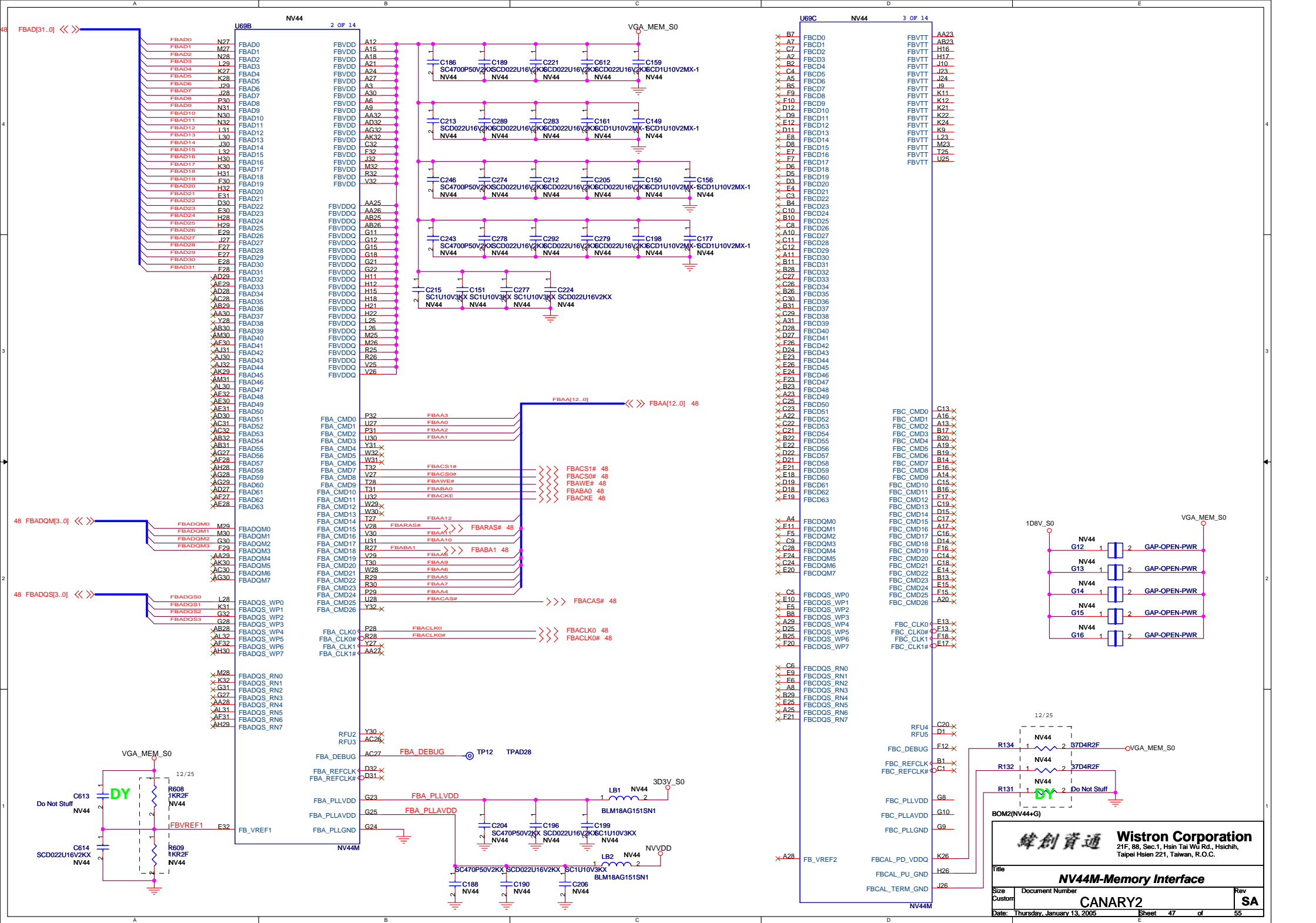
BOM2(NV44+G)

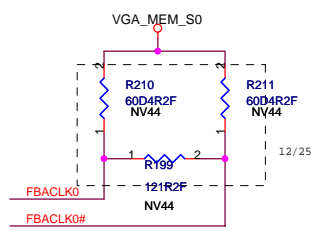
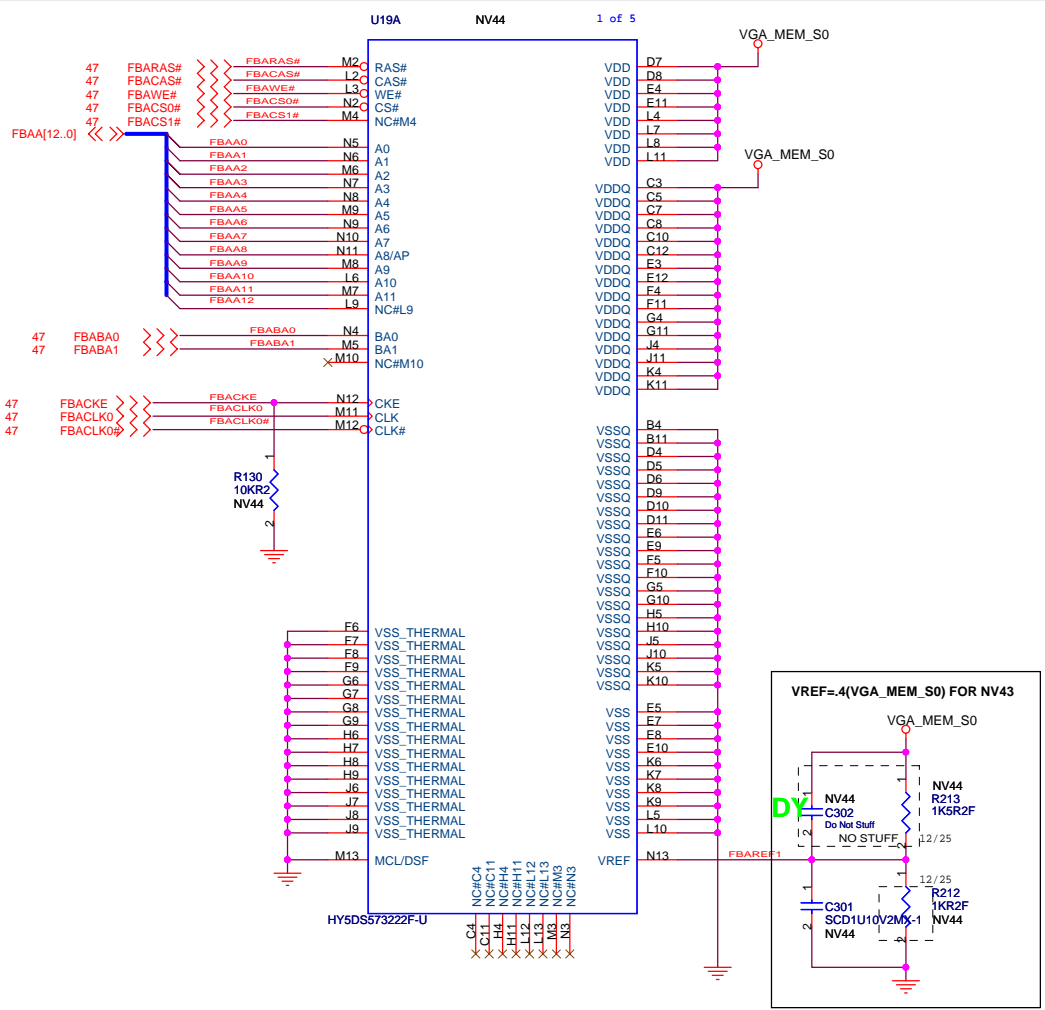
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	FAN5234_VGA_CORE_1D20V or 1D15V
-------	--

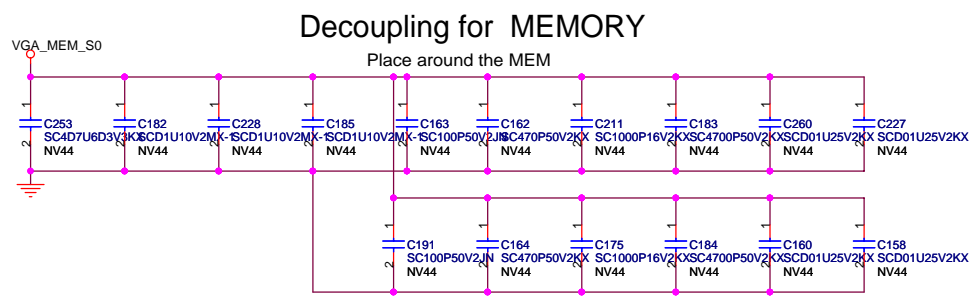
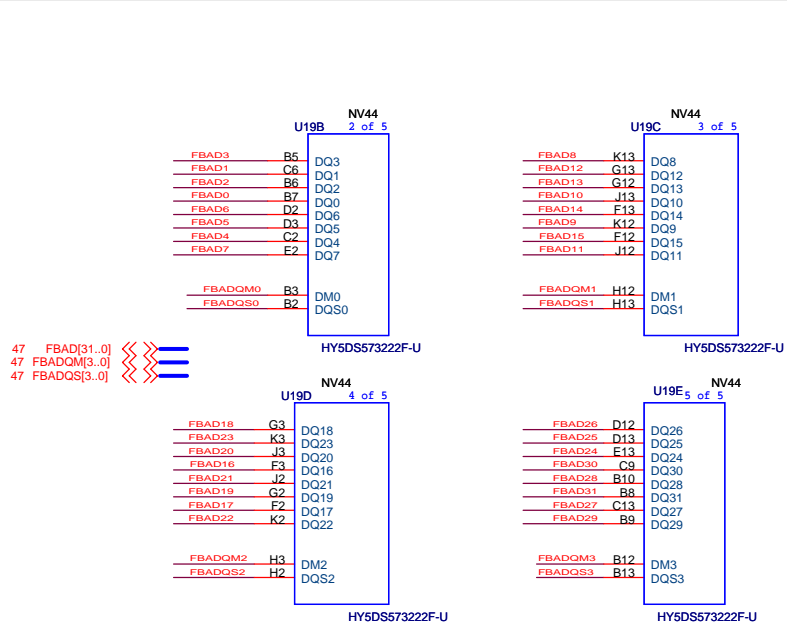
Size A3	Document Number CANARY2	Rev SA
Date: Thursday, January 13, 2005	Sheet 45 of 55	

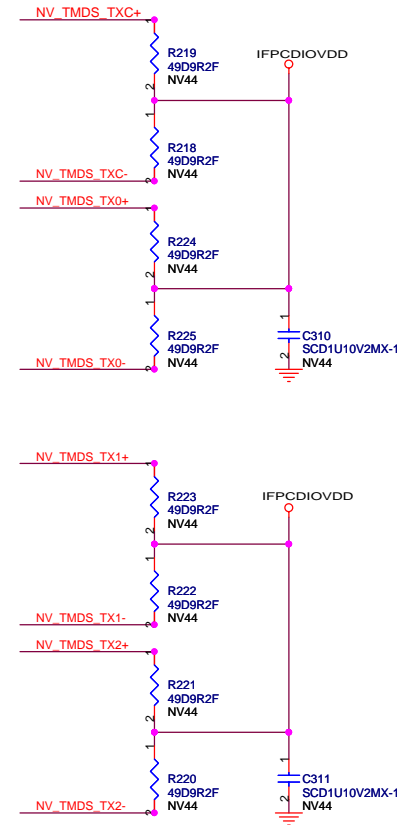
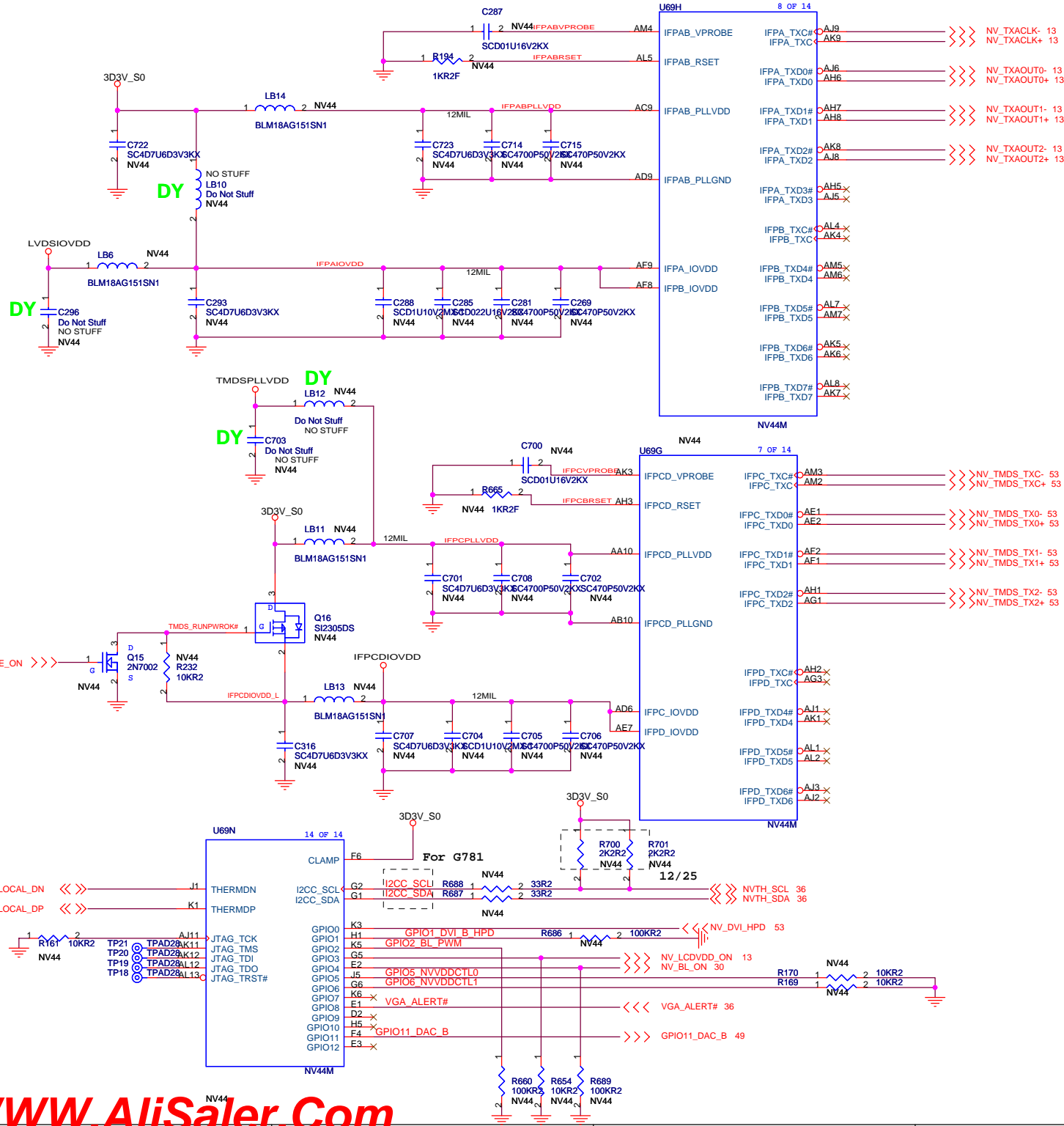


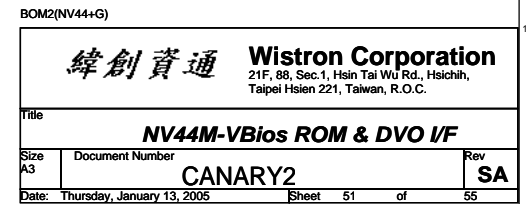


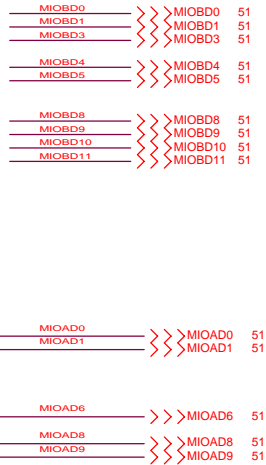


Must be placed as close as possible to minimize the stub length!!









STRAP BIT	LOGIC 0	LOGIC 1	REG: NV_STRAP_0
0			PCI_AD_SWAP 0: REVERSED 1: NORMAL DEFAULT
1	NV37 NV4x	MIOAD1 R202 1 NV44 2KR2	SUB_VENDOR 0: SYSTEM BIOS DEFAULT 1: ADAPTER BIOS
2		R67A NV44 Do Not Stuff NO STUFF MIOBD0 R676 1 NV44 2KR2	RAM_CFG_0 MS_0001: 8Mx32 DDR Monolithic (128bit NV43 or 64bit NV44) DEFAULT
3		R674 NV44 Do Not Stuff NO STUFF MIOBD1 R675 1 NV44 Do Not Stuff NO STUFF	RAM_CFG_1 MS_1001: 8Mx32 DDR Monolithic (64bit NV43 or 32bit NV44)
4		R188 NV44 Do Not Stuff NO STUFF MIOBD8 R195 1 NV44 Do Not Stuff NO STUFF	RAM_CFG_2 MS_0011: 8Mx32 DDR Stacked Die 2x4MX32
5		R173 NV44 Do Not Stuff NO STUFF MIOBD9 R173 1 NV44 Do Not Stuff NO STUFF	RAM_CFG_3 MS_1110: 4Mx32 DDR Generic (128bit NV43 or 64bit NV44)
6			CRYSTAL_CFG[1:0] MS_00: 13.5MHz MS_01: 14.318MHz MS_10: 27MHz MS_11: RESERVED DEFAULT
22			CRYSTAL_0 CRYSTAL_1
7			TV_MODE_CFG[1:0] MS_00: SECAM MS_01: NTSC MS_10: PAL MS_11: VGA DEFAULT
8			TV_MODE_0 TV_MODE_1
9			AGP8x/4x 0: 8x 1: 4x DEFAULT
10			AGP_SIDEBAND 0: ENABLE 1: DISABLE DEFAULT
11			AGP_FASTWRITE 0: ENABLE 1: DISABLE DEFAULT
12		R679 2KR2 2 NV44 MIOBD4 R679 Do Not Stuff NO STUFF	PCI_DEVID_0
13		R683 2KR2 2 NV44 MIOBD5 R683 Do Not Stuff NO STUFF	PCI_DEVID_1
20		R689 2KR2 2 NV44 MIOBD3 R689 Do Not Stuff NO STUFF	PCI_DEVID_2
21		R174 Do Not Stuff NO STUFF MIOBD11 R175 2KR2 2 NV44	PCI_DEVID_3
14			BUS_TYPE 0: PCI 1: AGP DEFAULT
29		MIOBD10 R187 2KR2 2 NV44	ROM_TYPE_0
30		R673 2KR2 2 NV44 MIOB_VSYNC >>> MIOB_VSYNC 51	ROM_TYPE_1 MS_00: PARALLEL MS_01: SERIAL AT25F MS_10: SERIAL SST45VF MS_11: RESERVED DEFAULT
REG: NV_STRAP_1			
11		R209 2KR2 2 NV44 MIOAD0 R209 Do Not Stuff NO STUFF	PEX_PLL_EN_TERM100
12		R199 Do Not Stuff NO STUFF MIOAD6 R199 2KR2 2 NV44	3GIO_PADCFG_LUT_ADR[0]
13		R203 2KR2 2 NV44 MIOAD8 R204 Do Not Stuff NO STUFF	3GIO_PADCFG_LUT_ADR[1]
14		R208 2KR2 2 NV44 MIOAD9 R205 Do Not Stuff NO STUFF	3GIO_PADCFG_LUT_ADR[2]

BOM2(NV44+G)

緯創資通

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Title

NV44M-Strap Pins

Size A3

Document Number

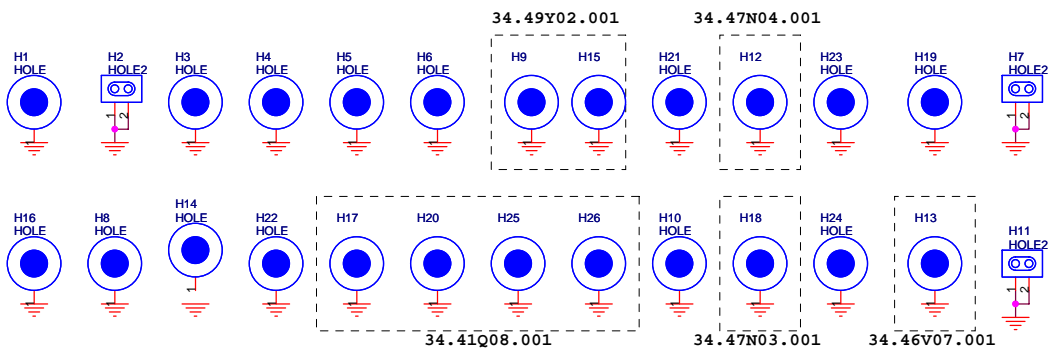
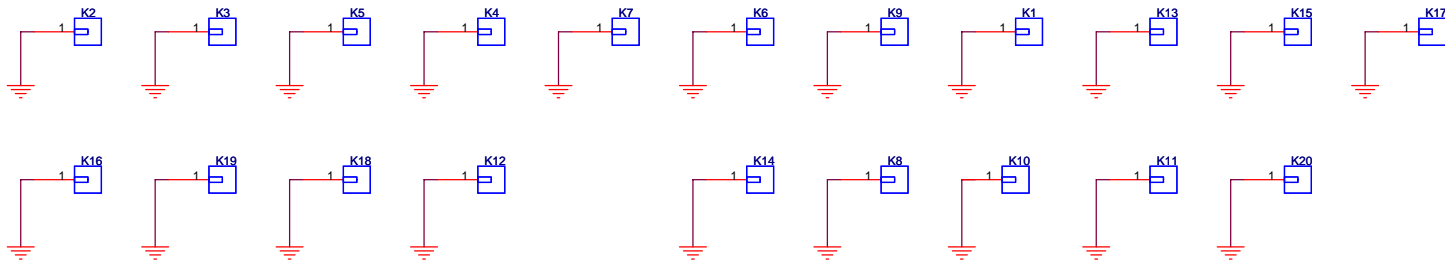
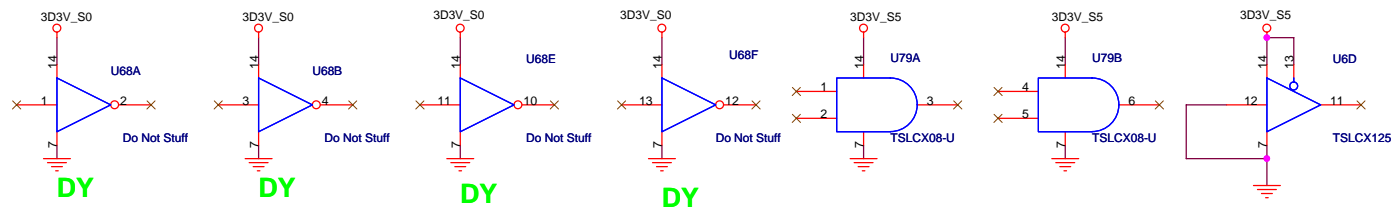
CANARY2

Rev

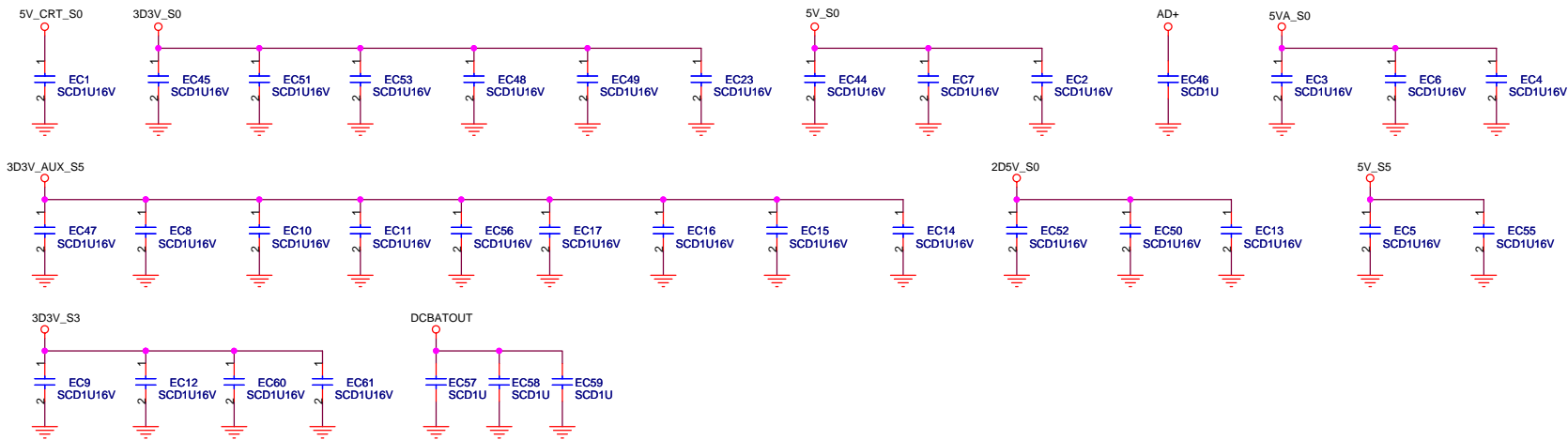
SA

Date: Monday, January 17, 2005

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BYPASS CAP



CROSS PLANE CAP